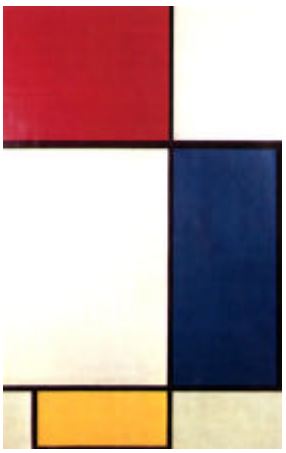
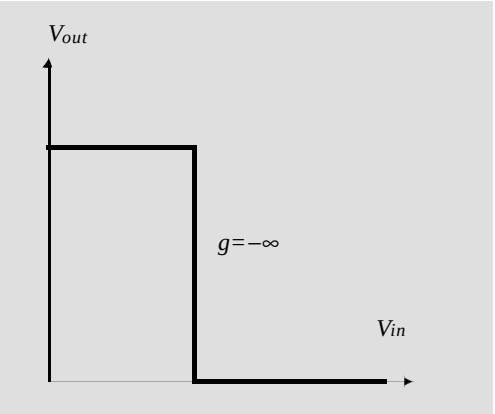
CMOS INVERTER



DIGITAL GATES
Fundamental Parameters

- Functionality
- Reliability, Robustness
- Area
- Performance
  - » Speed (delay)
  - » Power Consumption
  - » Energy

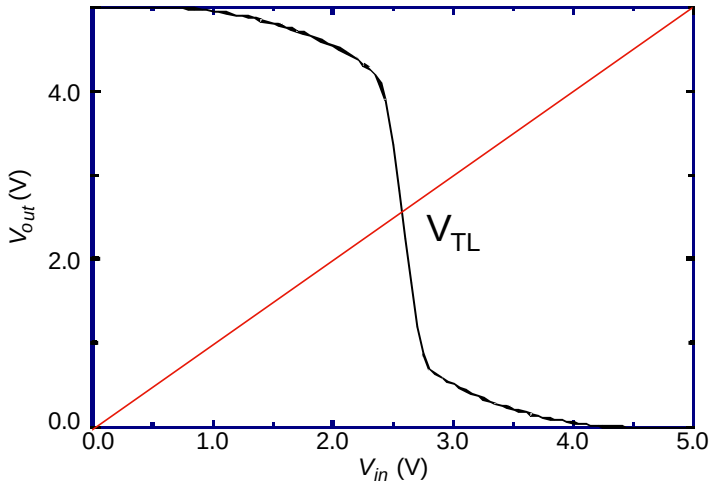
The Ideal Gate



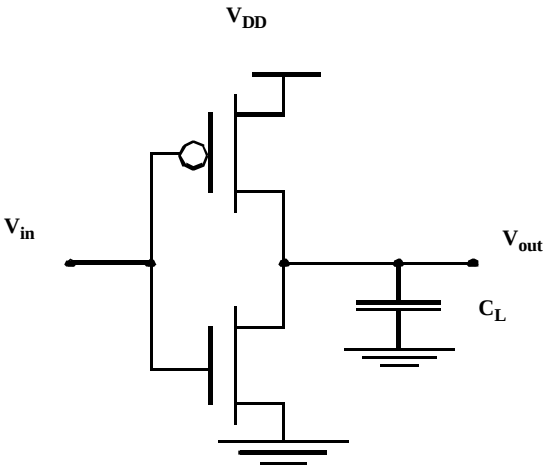
$R_i = \infty$

$R_o = 0$

VTC of Real Inverter



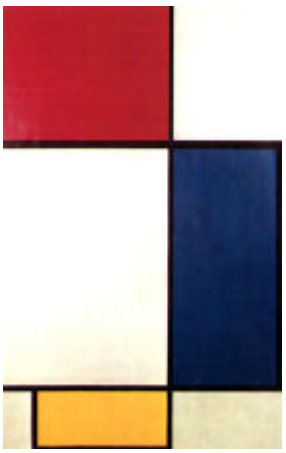
The CMOS Inverter: A First Glance



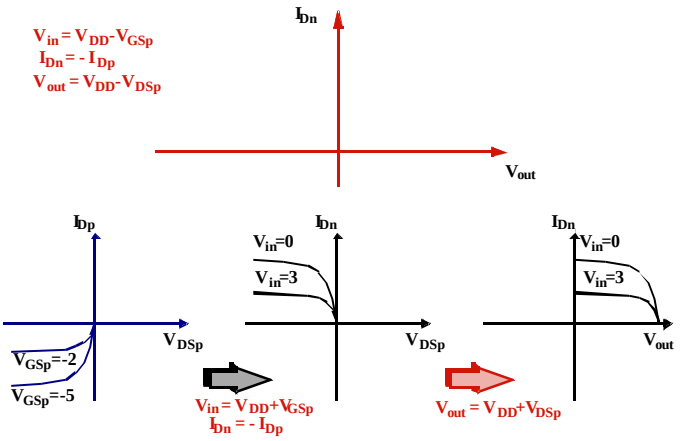
CMOS Properties

- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching

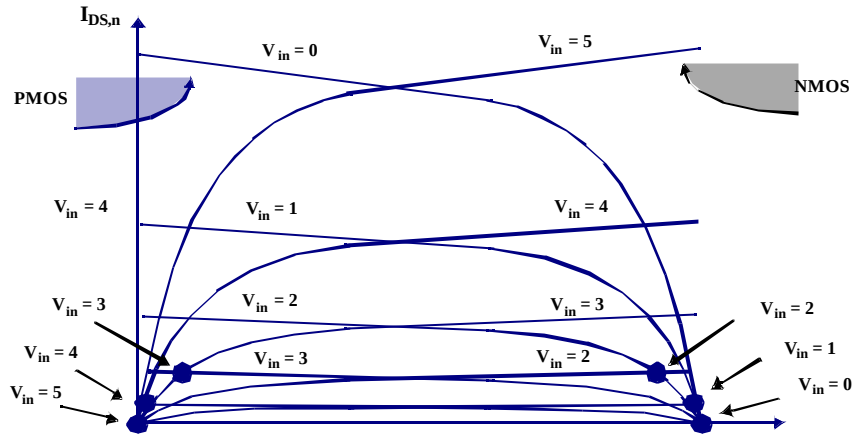
Voltage Transfer Characteristic



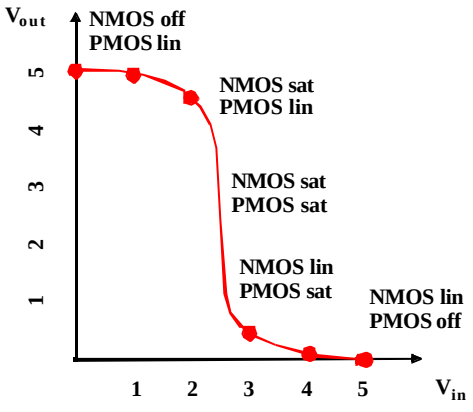
PMOS Load Lines



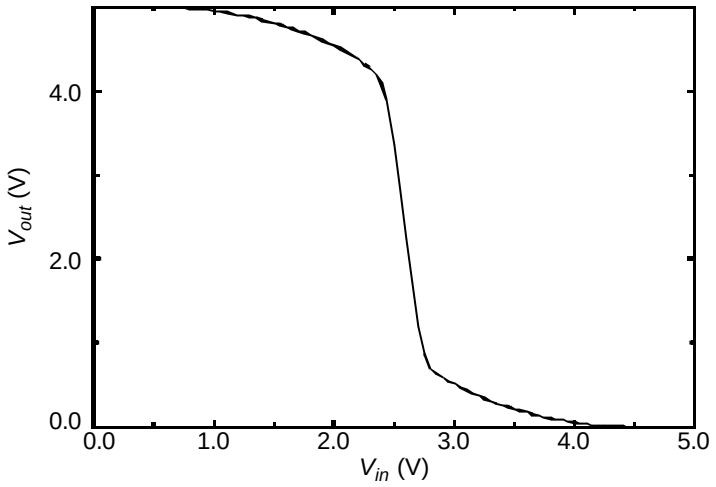
CMOS Inverter Load Characteristics



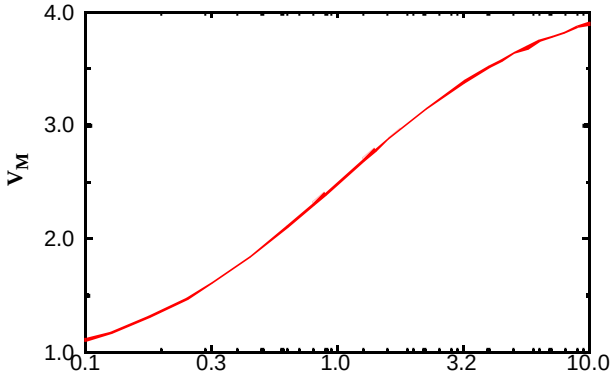
CMOS Inverter VTC



Simulated VTC

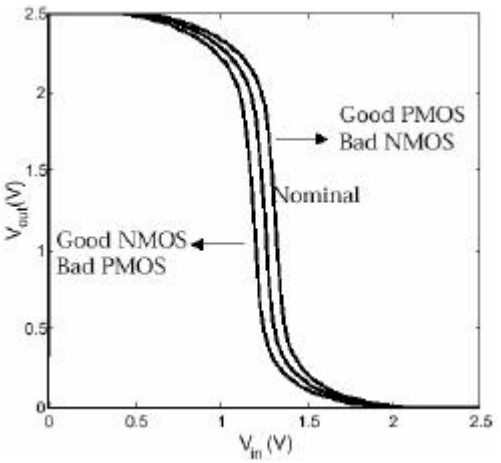


Gate Switching Threshold

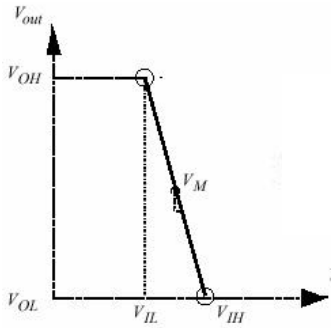


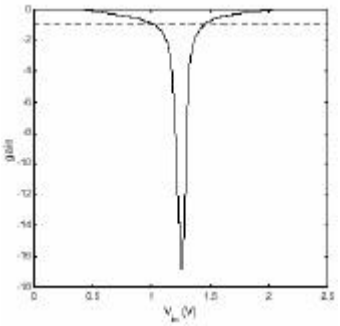
$$V_M = \frac{r(V_{DD} - |V_{Tp}|) + V_{Tn}}{1 + r} \quad \text{with} \quad r = \sqrt{\frac{k_p}{k_n}}$$

Impact of process variations



V_{IH}, V_{IL} and gain

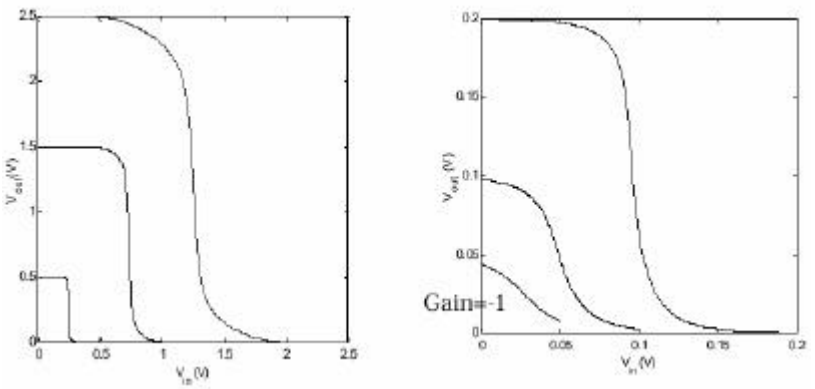




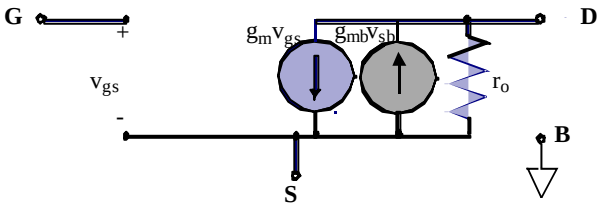
$$V_{IH} = V_M + \frac{V_M}{g}$$

$$V_{IL} = V_M - \frac{V_{DD} - V_M}{g}$$

Gain as a function of V_{DD}



MOS Transistor Small Signal Model

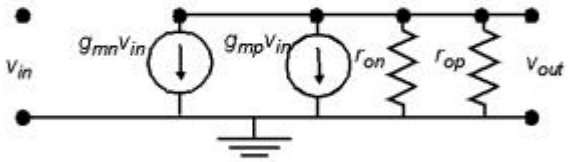


	g_m	r_0	g_{mb}
LIN	kV_{DS}	$\frac{1}{k(V_{GS} - V_T - V_{DS})}$	$\frac{0.5 g_m \gamma}{\sqrt{2\Phi_F + V_{SB}}}$
SAT	$k(V_{GS}-V_T)(1+\lambda V_{DS})$	$\frac{1+\lambda V_{DS}}{\lambda I_{DS}}$	

Determining V_{IH} and V_{IL}

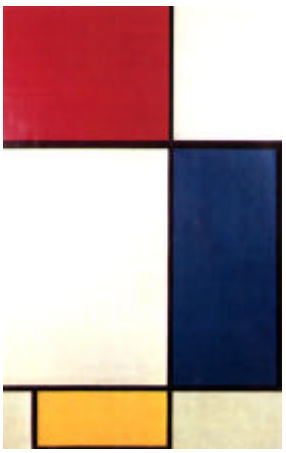
At V_{IH} (V_{IL}): $\frac{\partial V_{out}}{\partial V_{in}} = -1$

small-signal model of inverter

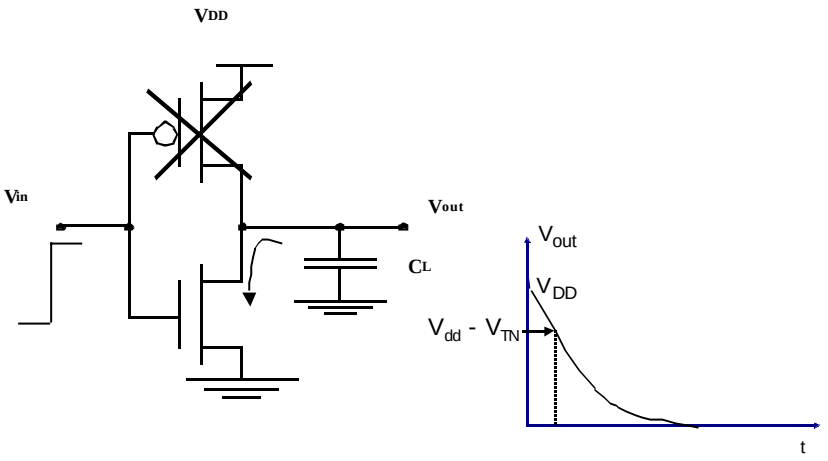


$$g = \frac{v_{out}}{v_{in}} = -(g_{mn} + g_{mp}) \times (r_{on} \| r_{op}) = -1$$

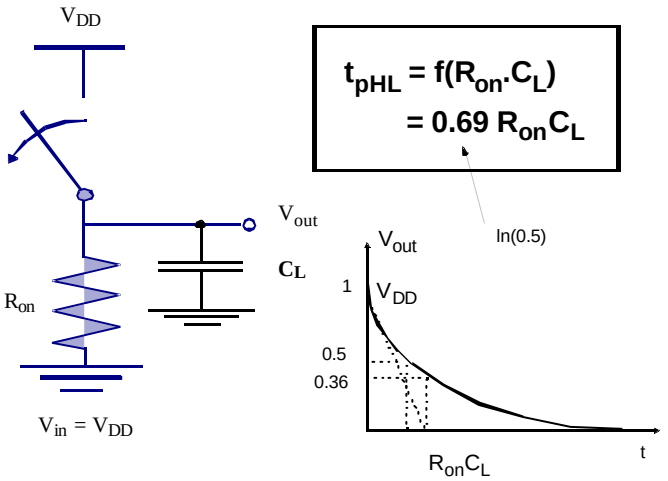
Propagation Delay



Computing CMOS inverter delay in the quadratic model

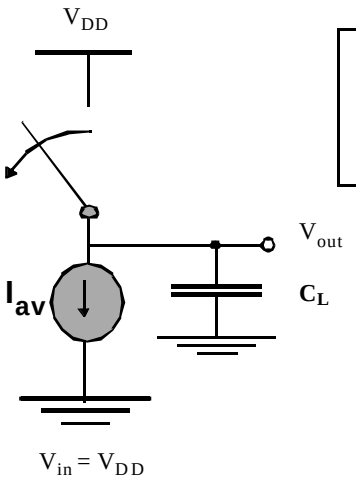


Computing CMOS inverter delay in the linear model



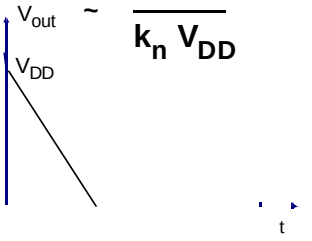
$$t_{pHL} = f(R_{on}.C_L) = 0.69\ R_{on}C_L$$

Computing CMOS inverter delay in the constant model

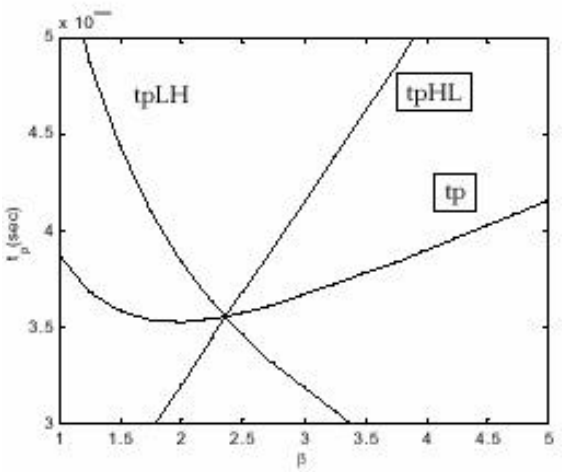


$$t_{pHL} = \frac{C_L V_{swing}/2}{I_{av}}$$

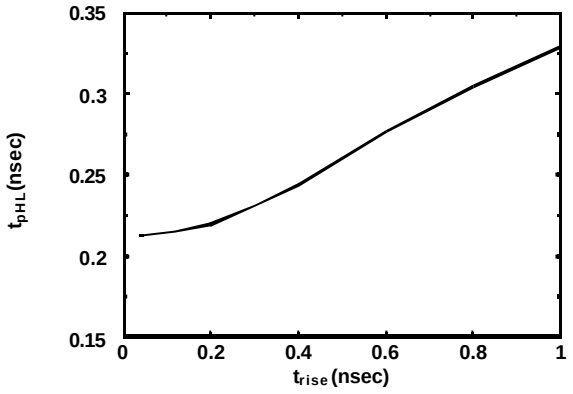
$$V_{out} \sim \frac{C_L}{k_n V_{DD}}$$



NMOS / PMOS ratio

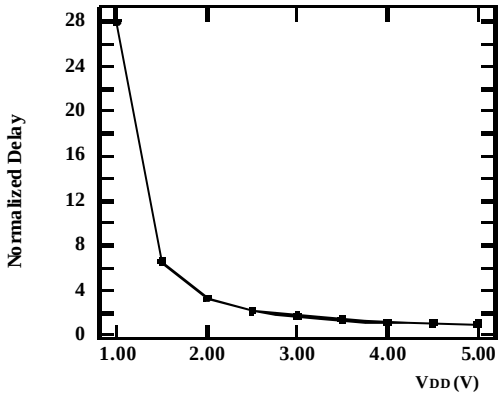


Impact of Rise Time on Delay

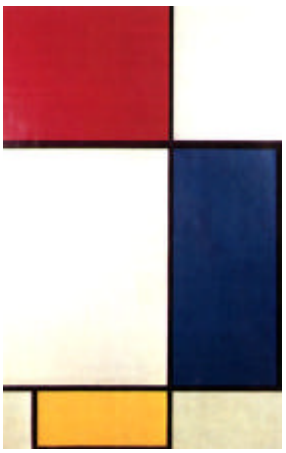


$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$

Delay as a function of V_{DD}



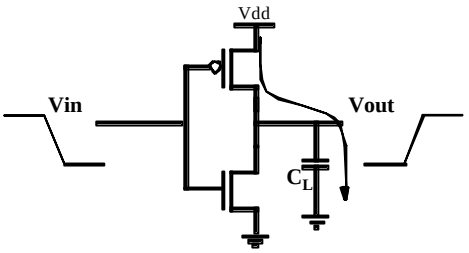
Power Consumption



Where Does Power Go in CMOS?

- **Dynamic Power Consumption**
  - » **Charging and Discharging Capacitors**
- **Short Circuit Currents**
  - » **Short Circuit Path between Supply Rails during Switching**
- **Leakage**
  - » **Leaking diodes and transistors**

Dynamic Power Dissipation

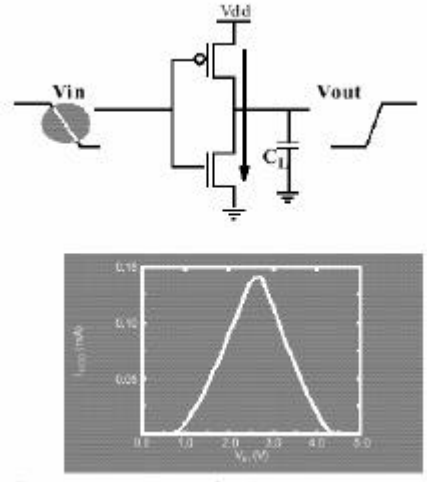


Energy/transition = $C_L * V_{dd}^2$

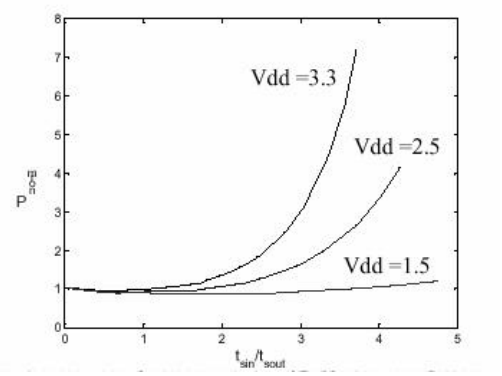
Power = Energy/transition * f = $C_L * V_{dd}^2 * f$

- **Not a function of transistor sizes!**
- **Need to reduce C_L, V_{dd}, and f to reduce power.**

Short circuit current

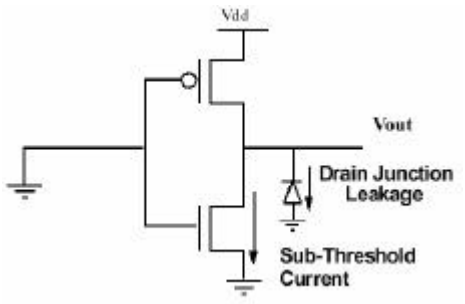


Minimizing SC Power



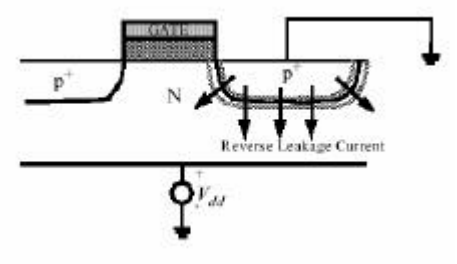
Keep the input and output fall time the same

Leakage (static) power



Sub-threshold current is one of the most Compelling issues in low-energy design

Reverse-biased diode leakage



- $J_S = J_S A$
- J_S=1-5pA/μm^2 in 1.2μm CMOS
- J_S doubles with every 9^{0}C in T

Sub-threshold leakage