CSE477
VLSI Digital Circuits
Spring 2004

Lecture 04: CMOS Inverter (static view)

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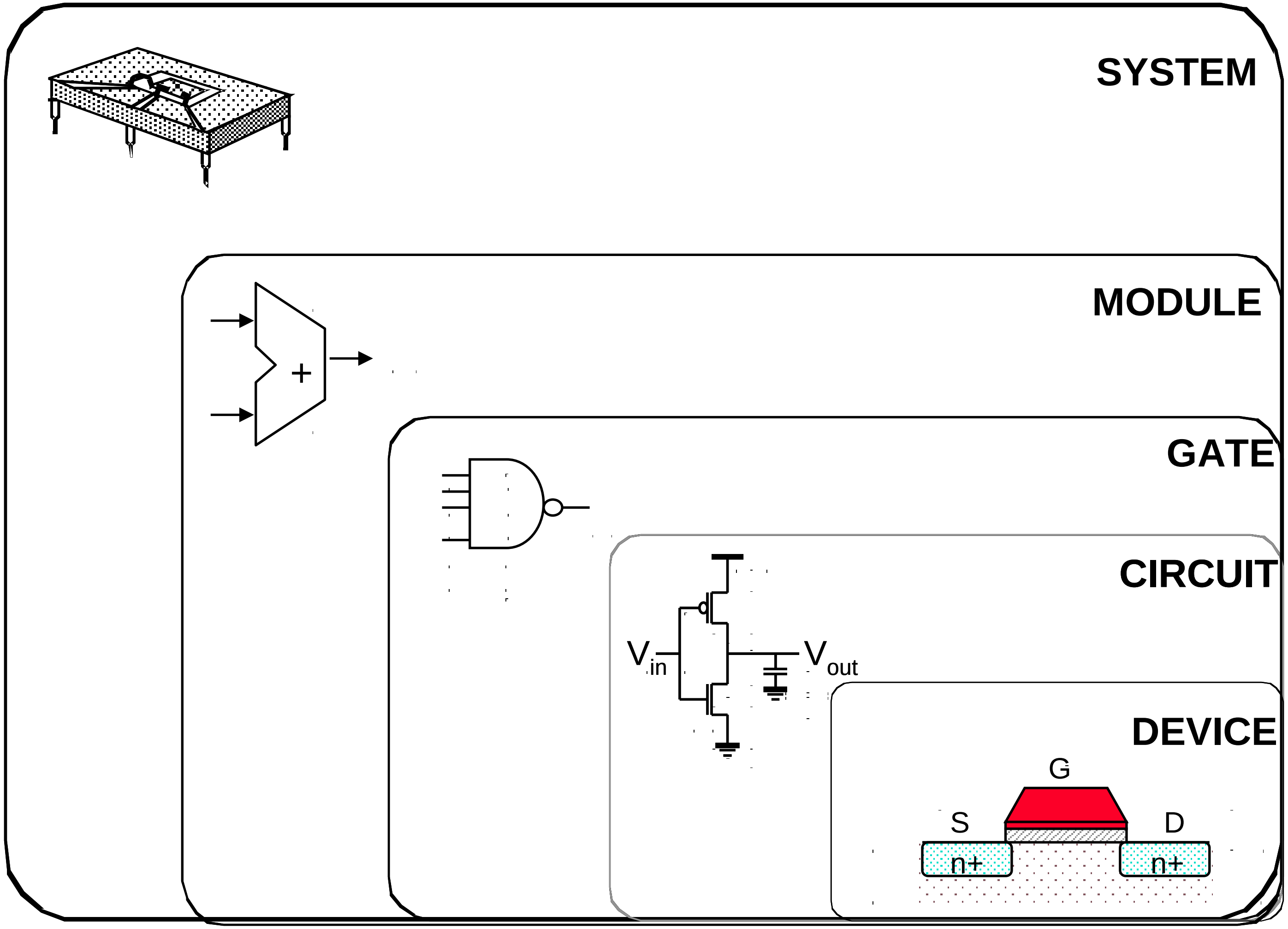
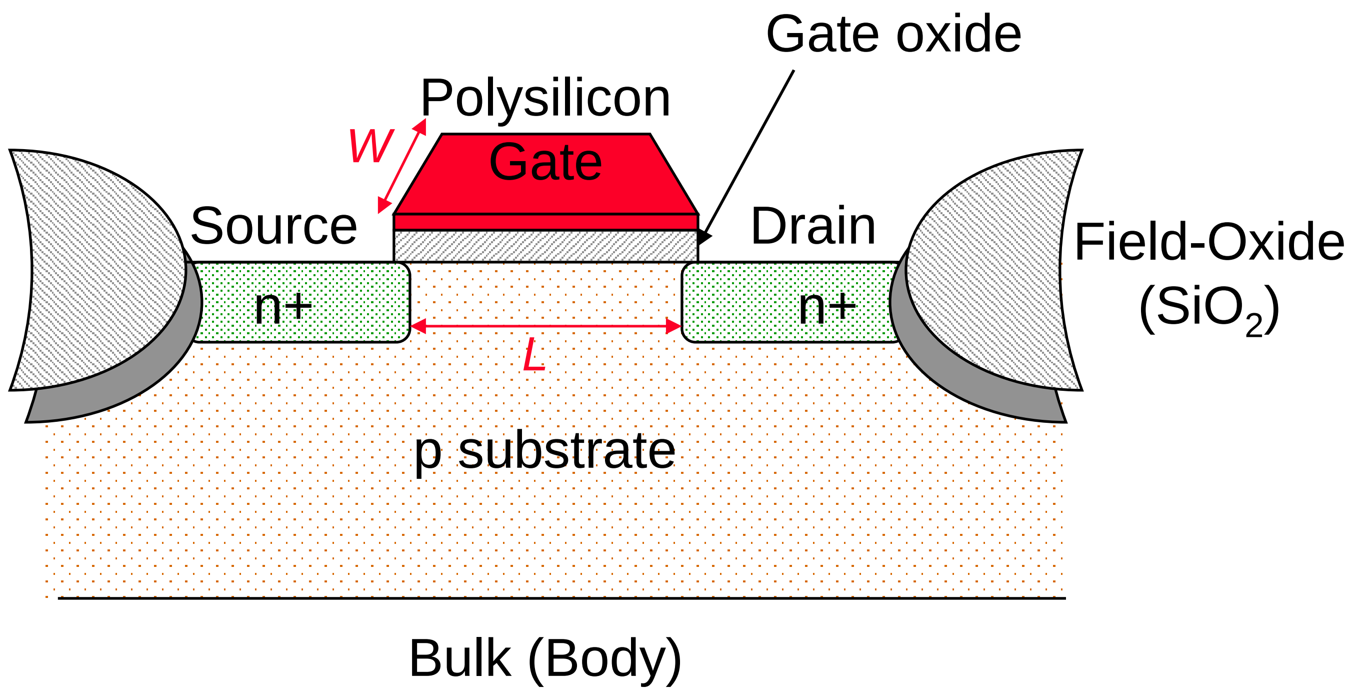
[Adapted from Rabaey's *Digital Integrated Circuits*, Second Edition, ©2003
J. Rabaey, A. Chandrakasan, B. Nikolic]

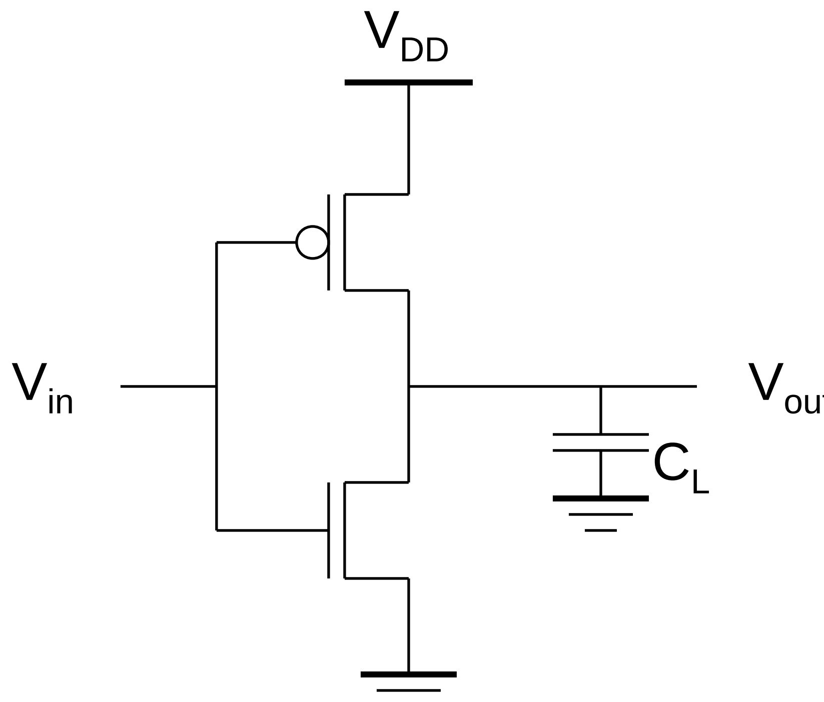
Review: Design Abstraction Levels



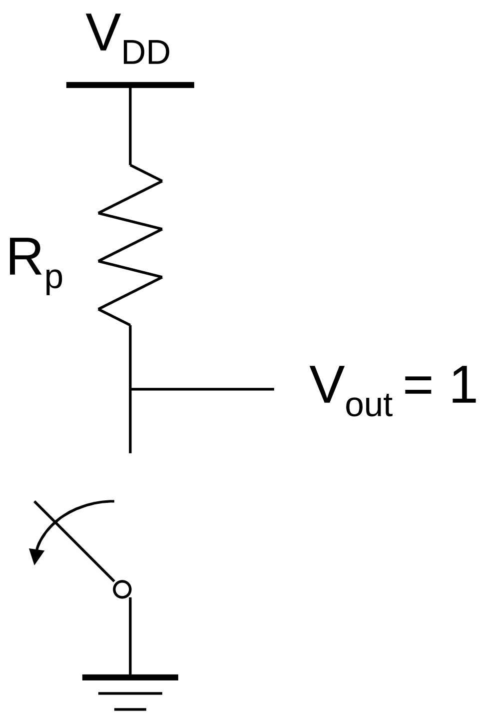
Review: The MOS Transistor



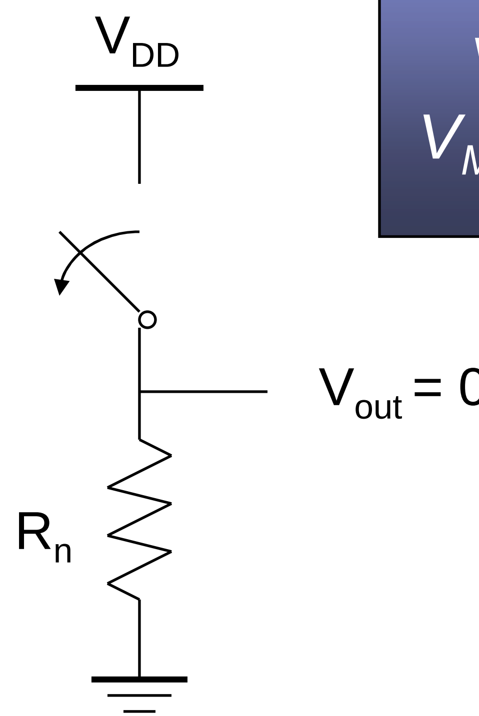
CMOS Inverter:
A First Look



CMOS Inverter:
Steady State Response



$V_{in} = 0$



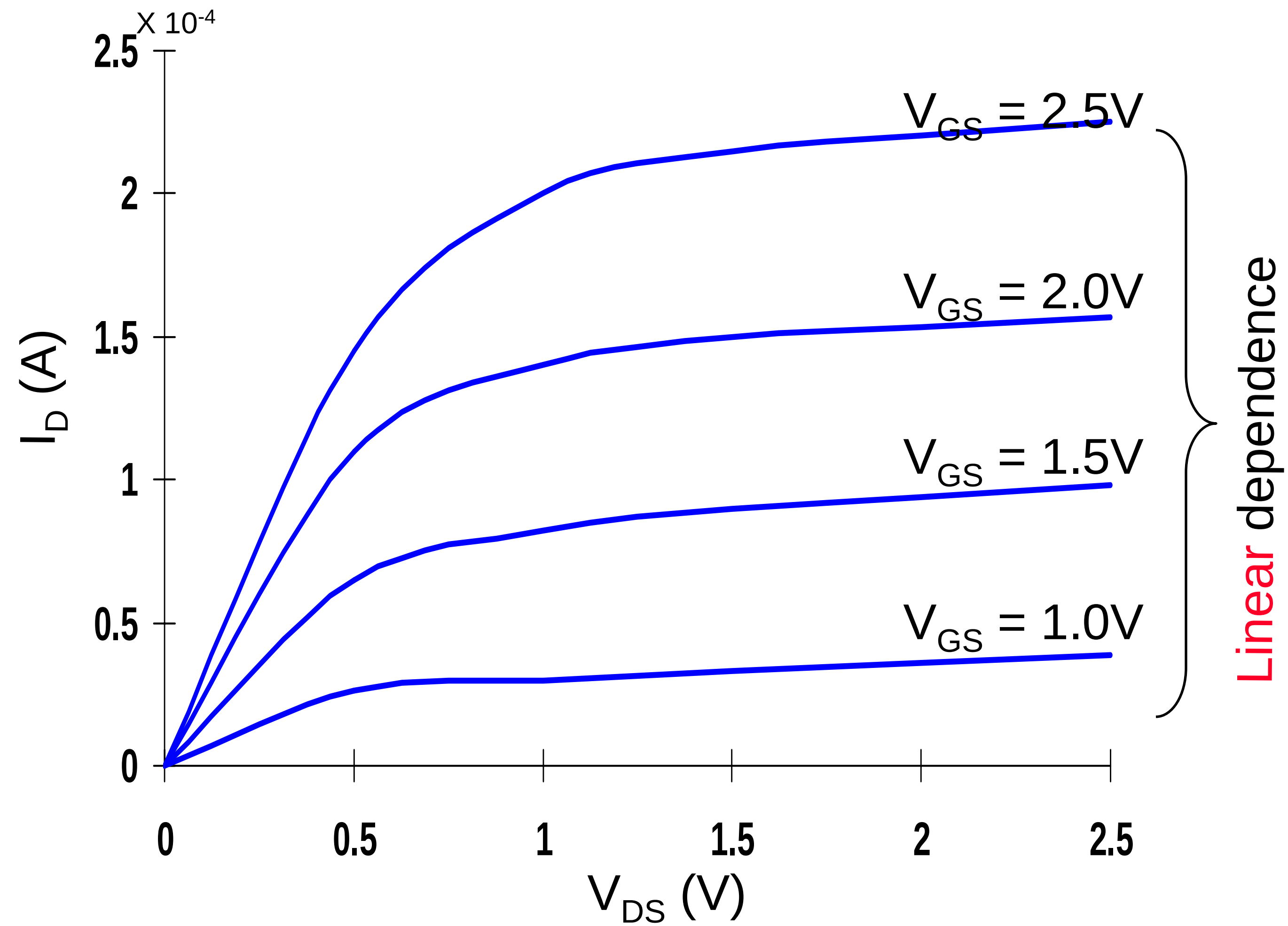
$V_{in} = V_{DD}$

$$V_{OL} = 0$$
$$V_{OH} = V_{DD}$$
$$V_M = f(R_n, R_p)$$

CMOS Properties

- Full rail-to-rail swing ⇒ high noise margins
  - Logic levels not dependent upon the relative device sizes ⇒ transistors can be minimum size ⇒ ratioless
- Always a path to V_{dd} or GND in steady state ⇒ low output impedance (output resistance in kΩ range) ⇒ large fan-out (albeit with degraded performance)
- Extremely high input resistance (gate of MOS transistor is near perfect insulator) ⇒ nearly zero steady-state input current
- No direct path steady-state between power and ground ⇒ no static power dissipation
- Propagation delay is a function of load capacitance and resistance of transistors

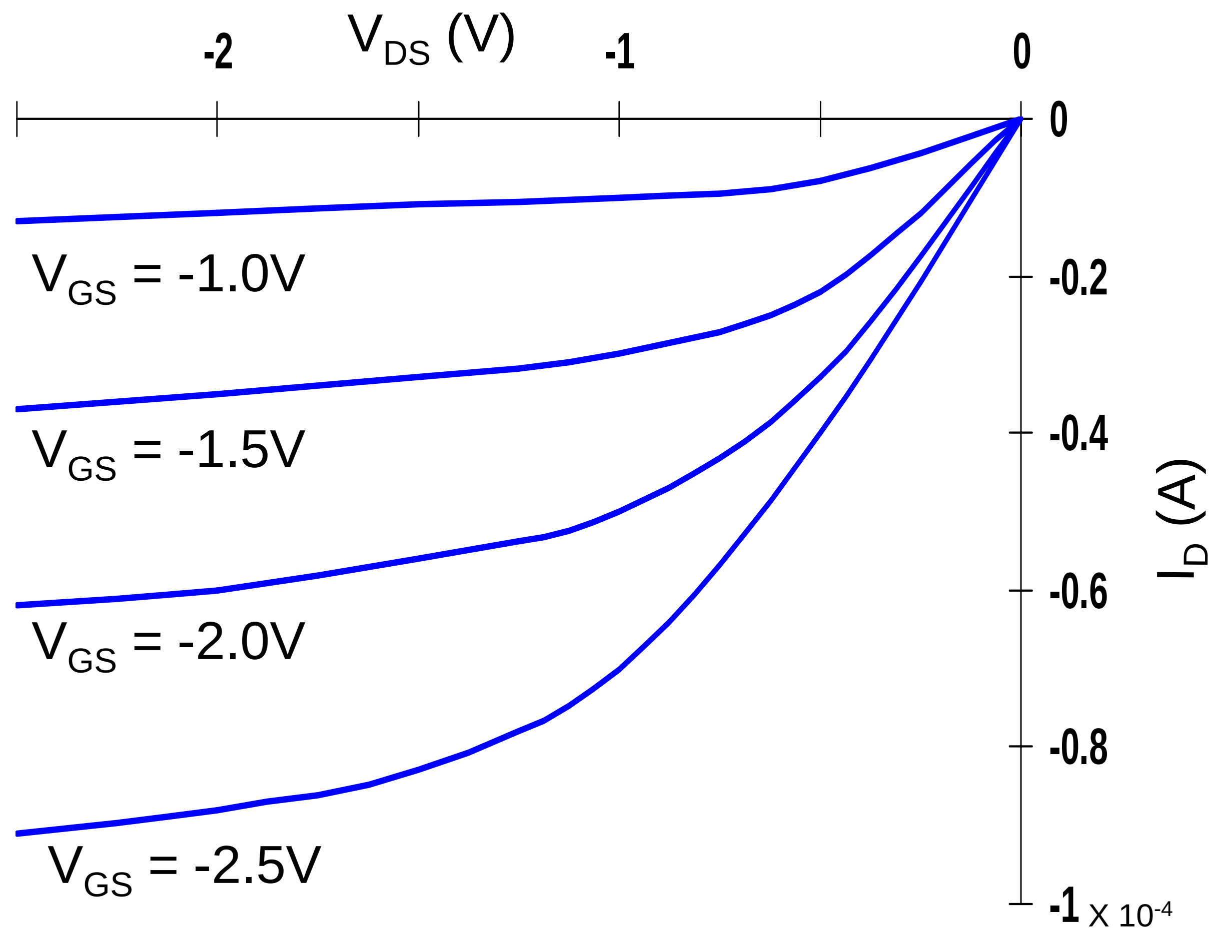
Review: Short Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

Review: Short Channel I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed



PMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = -0.4V

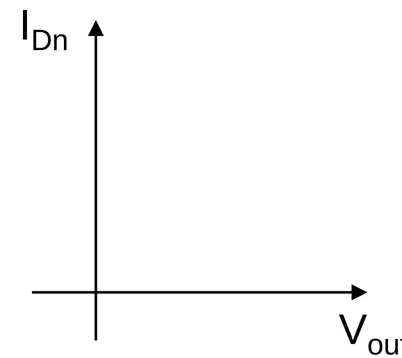
Transforming PMOS I-V Lines

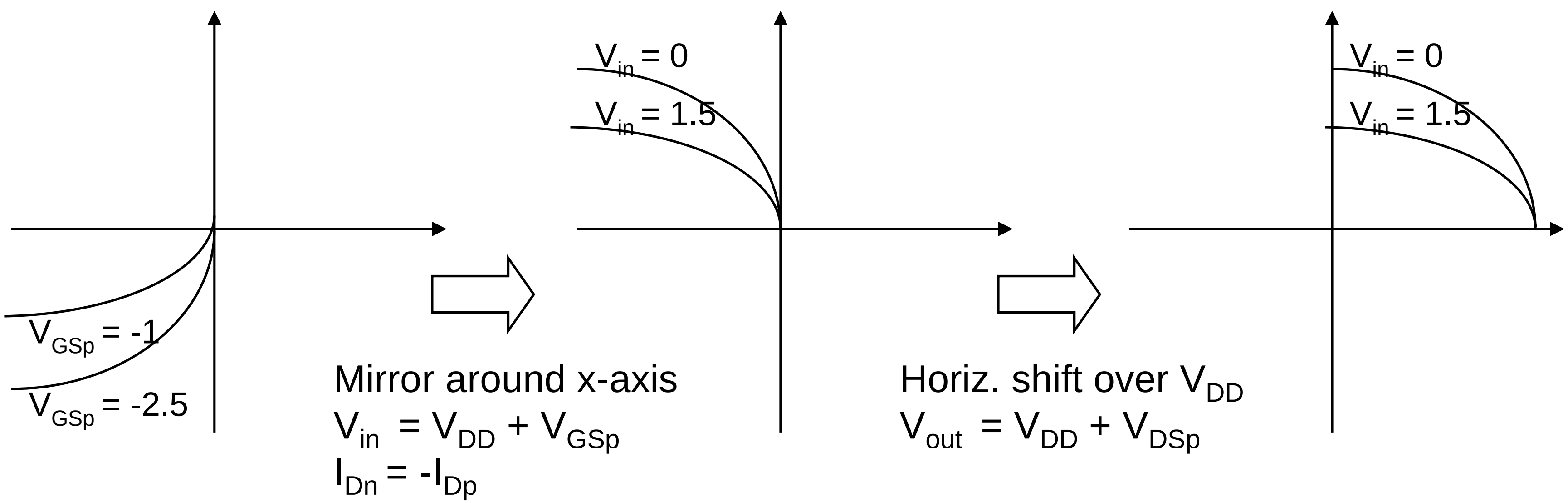
- Want common coordinate set V_{in}, V_{out}, and I_{Dn}

$I_{DSp} = -I_{DSn}$

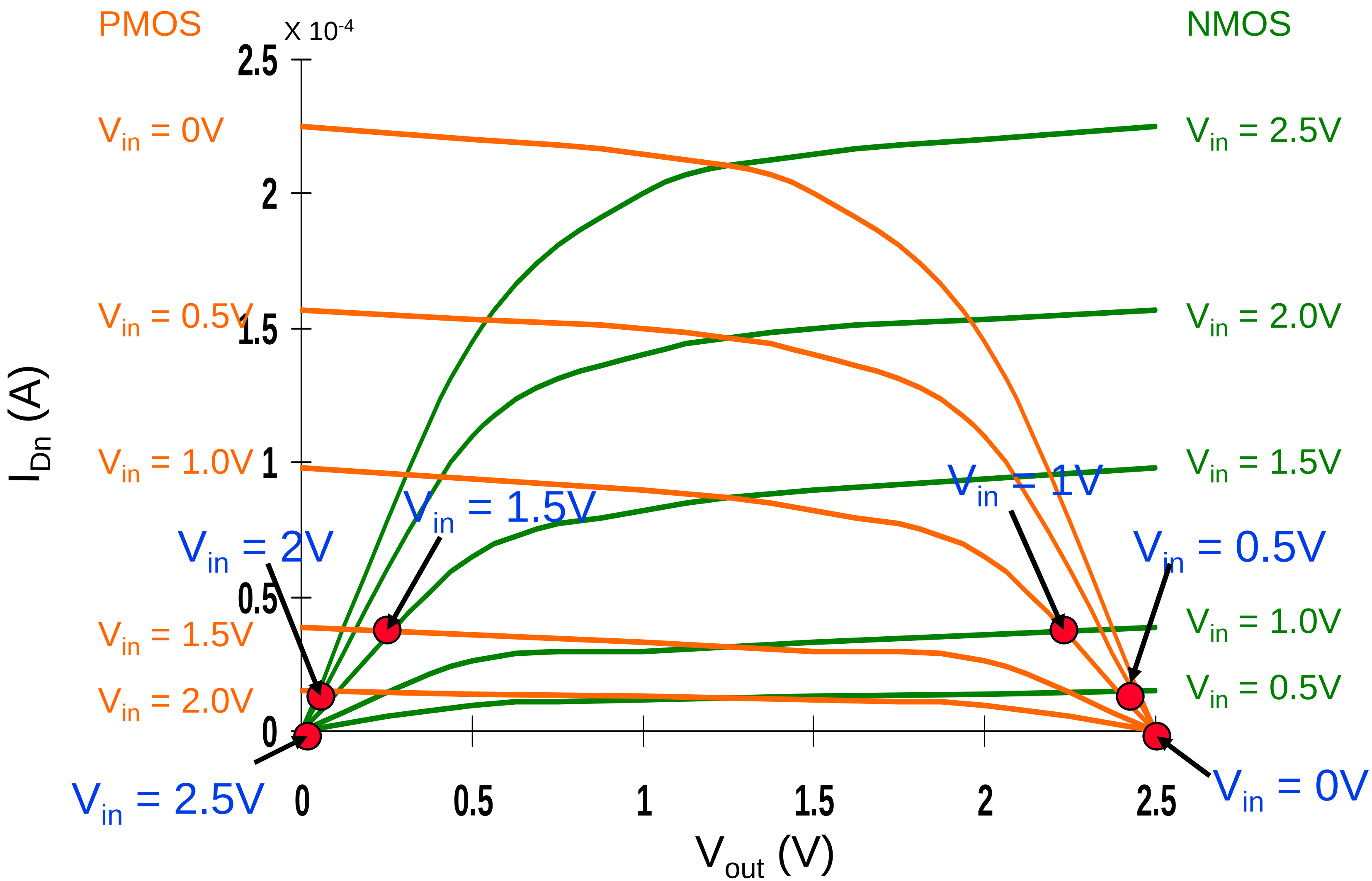
$V_{GSn} = V_{in}$; $V_{GSp} = V_{in} - V_{DD}$

$V_{DSn} = V_{out}$; $V_{DSp} = V_{out} - V_{DD}$



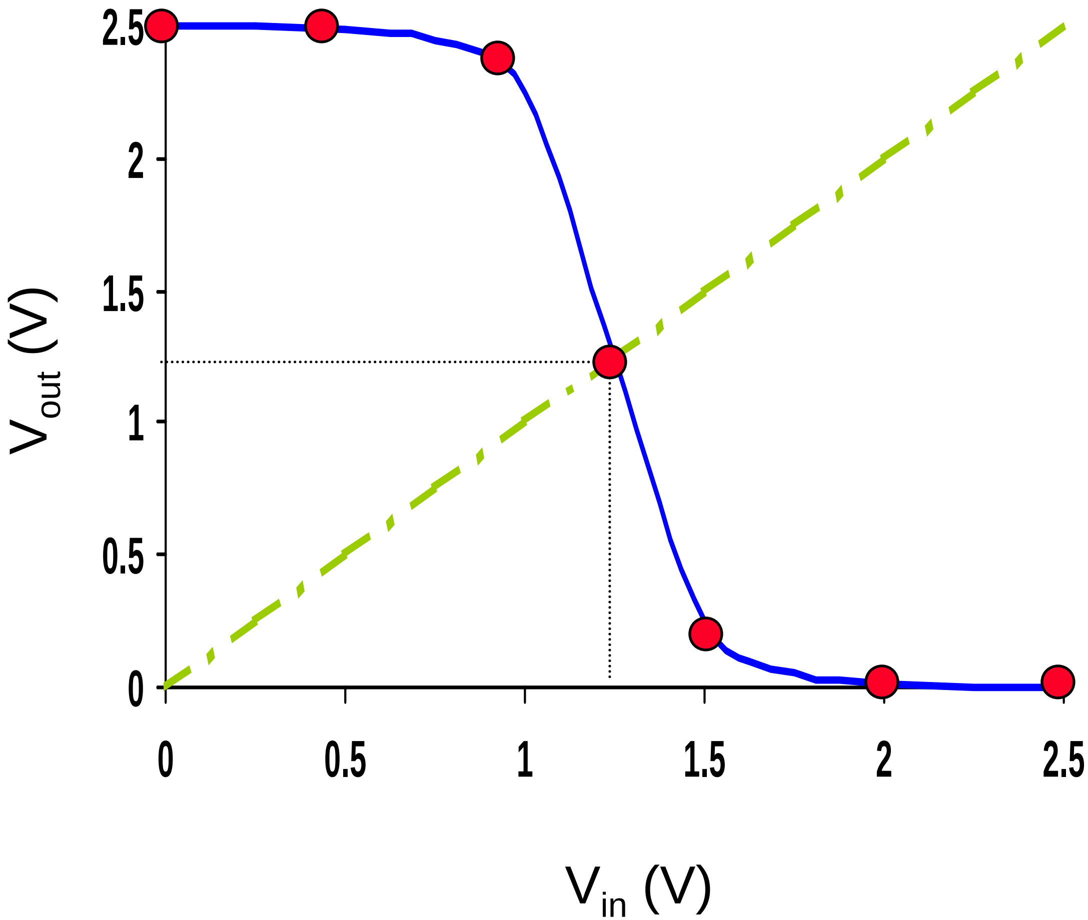


CMOS Inverter Load Lines

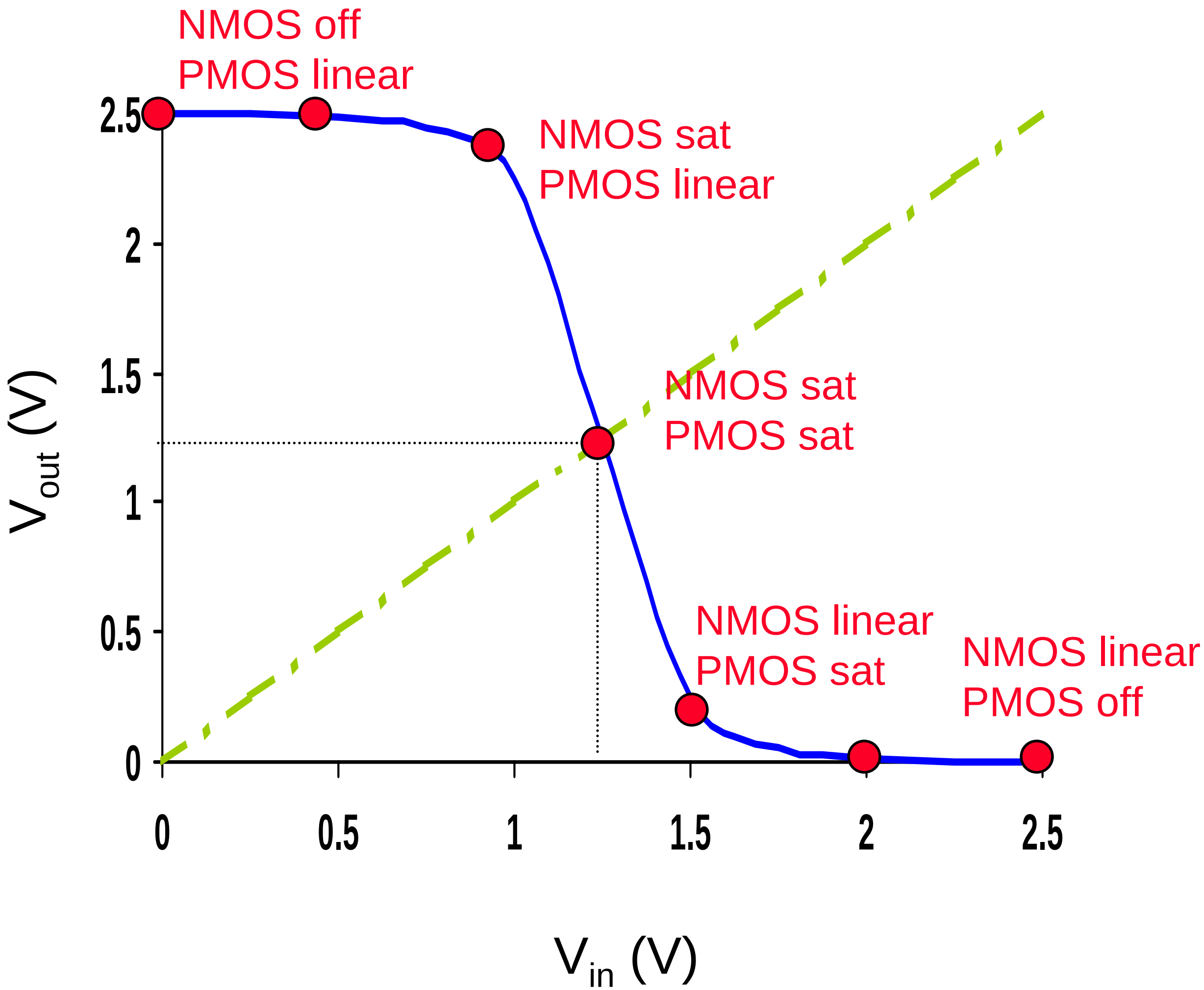


0.25um, W/L_n = 1.5, W/L_p = 4.5, V_{DD} = 2.5V, V_{Tn} = 0.4V, V_{Tp} = -0.4V

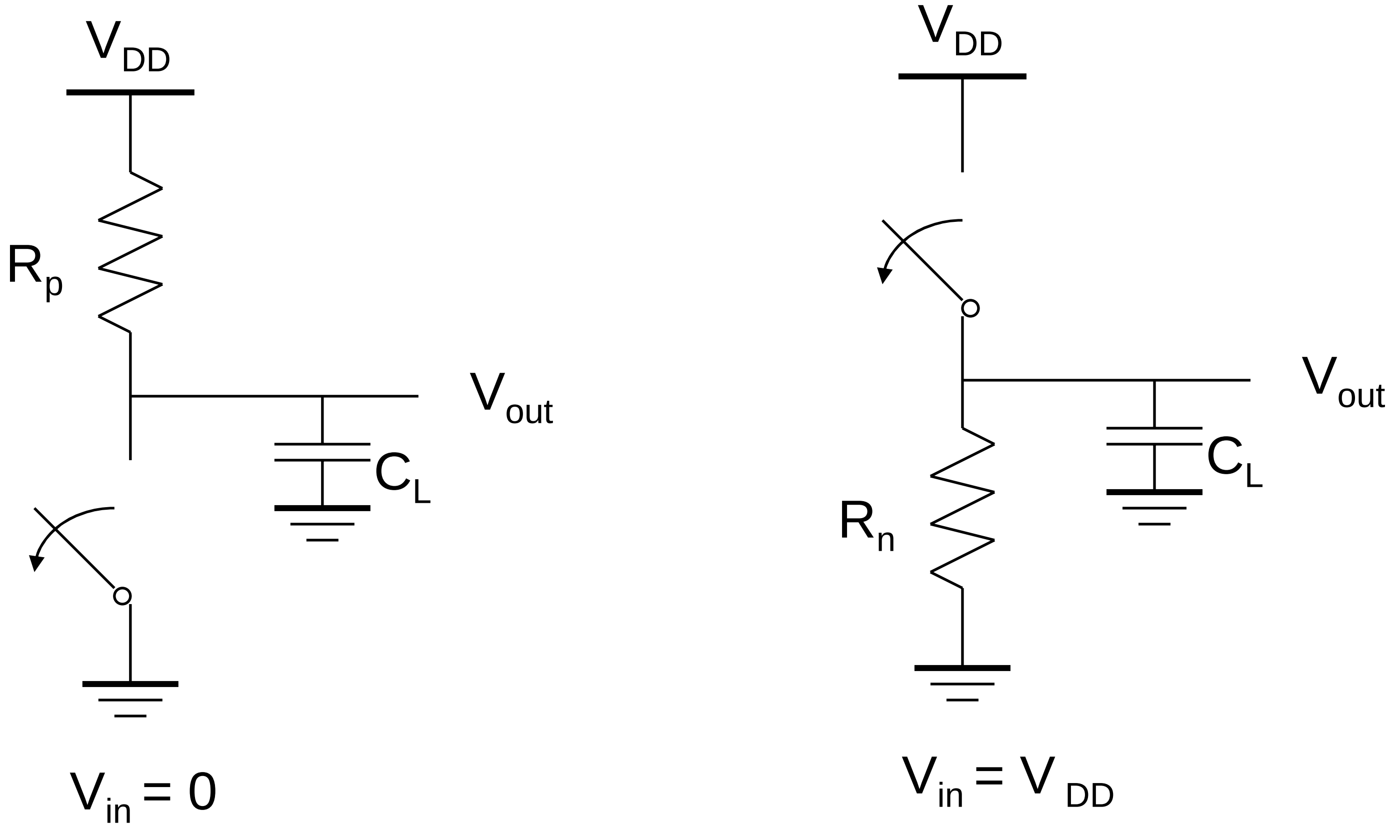
CMOS Inverter VTC



CMOS Inverter VTC



CMOS Inverter:
Switch Model of Dynamic Behavior



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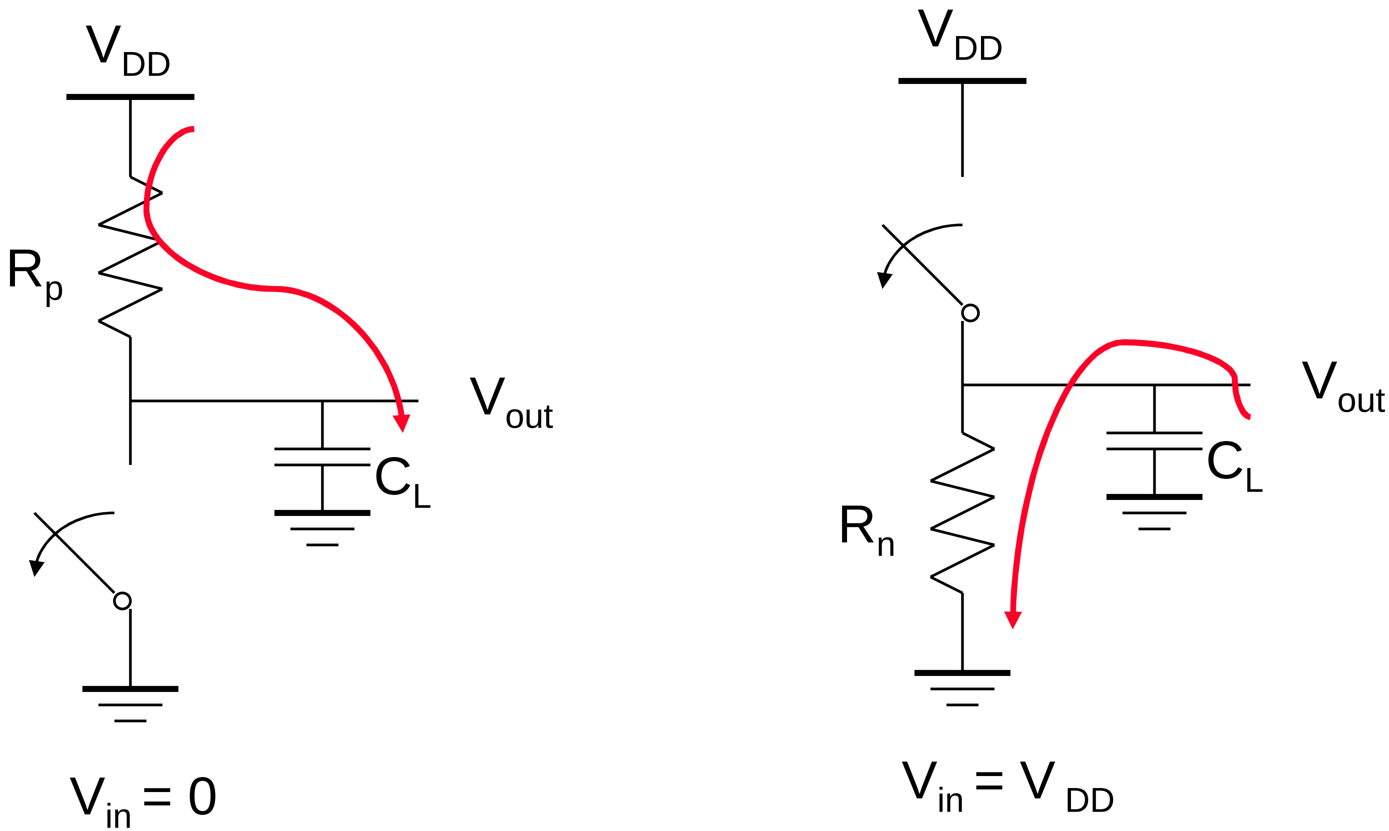

- Gate response time is determined by the time to charge C_L through R_p (discharge C_L through R_n)

Relative Transistor Sizing

- When designing static CMOS circuits, balance the driving strengths of the transistors by making the PMOS section wider than the NMOS section to
  - maximize the noise margins and
  - obtain symmetrical characteristics

Switching Threshold

- V_M where $V_{in} = V_{out}$ (both PMOS and NMOS in saturation since $V_{DS} = V_{GS}$)

$$V_M \approx rV_{DD}/(1 + r) \text{ where } r = k_p V_{DSATp}/k_n V_{DSATn}$$

- Switching threshold set by the ratio r, which compares the relative driving strengths of the PMOS and NMOS transistors

- Want $V_M = V_{DD}/2$ (to have comparable high and low noise margins), so want $r \approx 1$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n' V_{DSATn}(V_M - V_{Tn} - V_{DSATn}/2)}{k_p' V_{DSATp}(V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)}$$

Switch Threshold Example

- In our generic 0.25 micron CMOS process, using the process parameters from slide L03.26, a V_{DD} = 2.5V, and a 1.5 size NMOS device $(W/L)_n$

	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

$$\frac{(W/L)_p}{(W/L)_n} =$$

Switch Threshold Example

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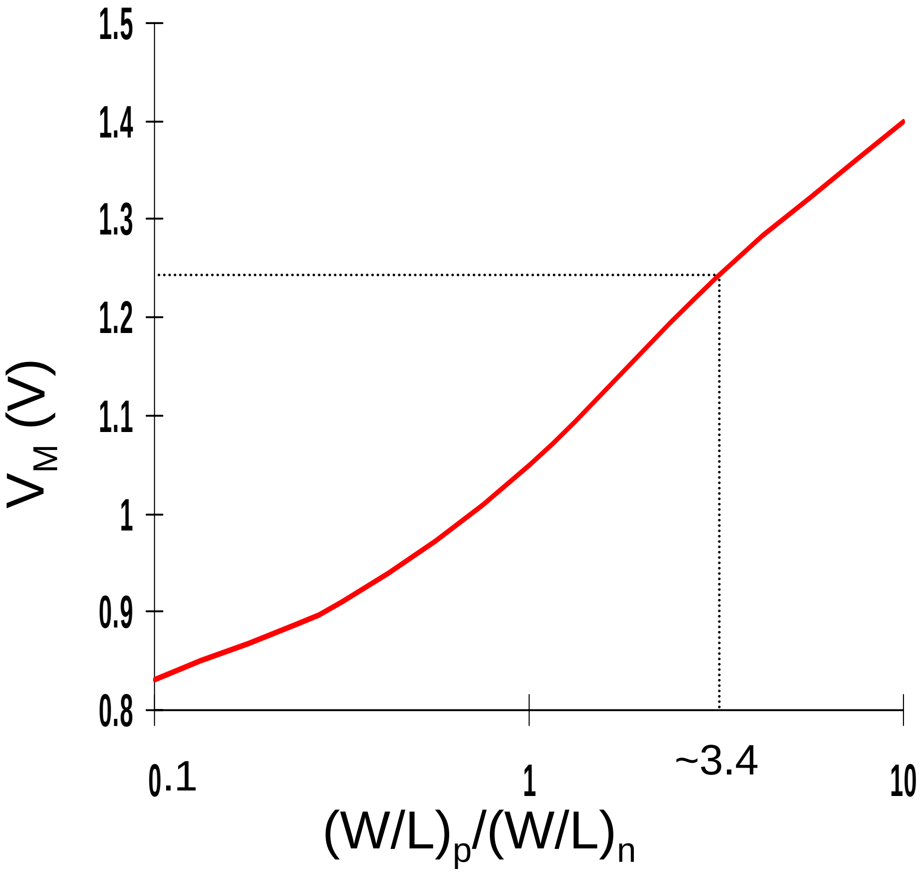
$$\frac{(W/L)_p}{(W/L)_n} = \frac{115 \times 10^{-6}}{-30 \times 10^{-6}} \times \frac{0.63}{-1.0} \times \frac{(1.25 - 0.43 - 0.63/2)}{(1.25 - 0.4 - 1.0/2)} = 3.5$$

$$(W/L)_p = 3.5 \times 1.5 = 5.25 \text{ for a } V_M \text{ of } 1.25V$$

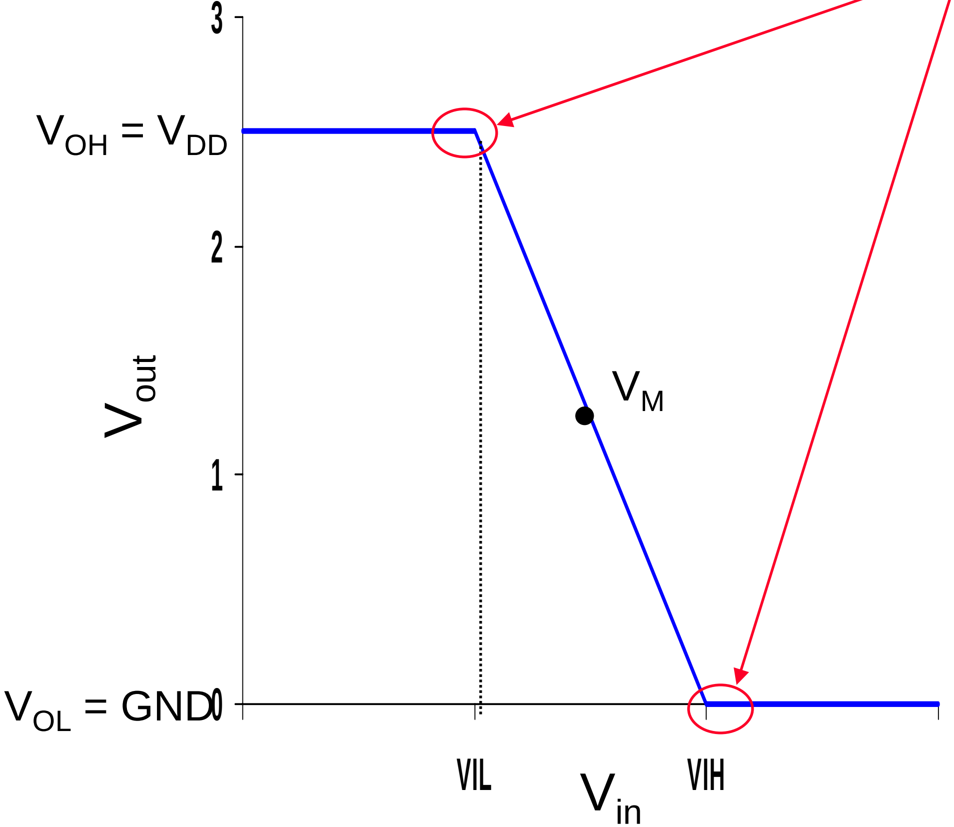
Simulated Inverter V_M



Note: x-axis is semilog

- V_M is relatively insensitive to variations in device ratio
  - setting the ratio to 3, 2.5 and 2 gives V_M's of 1.22V, 1.18V, and 1.13V
- Increasing the width of the PMOS moves V_M towards V_{DD}
- Increasing the width of the NMOS moves V_M toward GND

Noise Margins Determining V_{IH} and V_{IL}



A piece-wise linear approximation of VTC

By definition, V_{IH} and V_{IL} are where $dV_{out}/dV_{in} = -1$ (= gain)

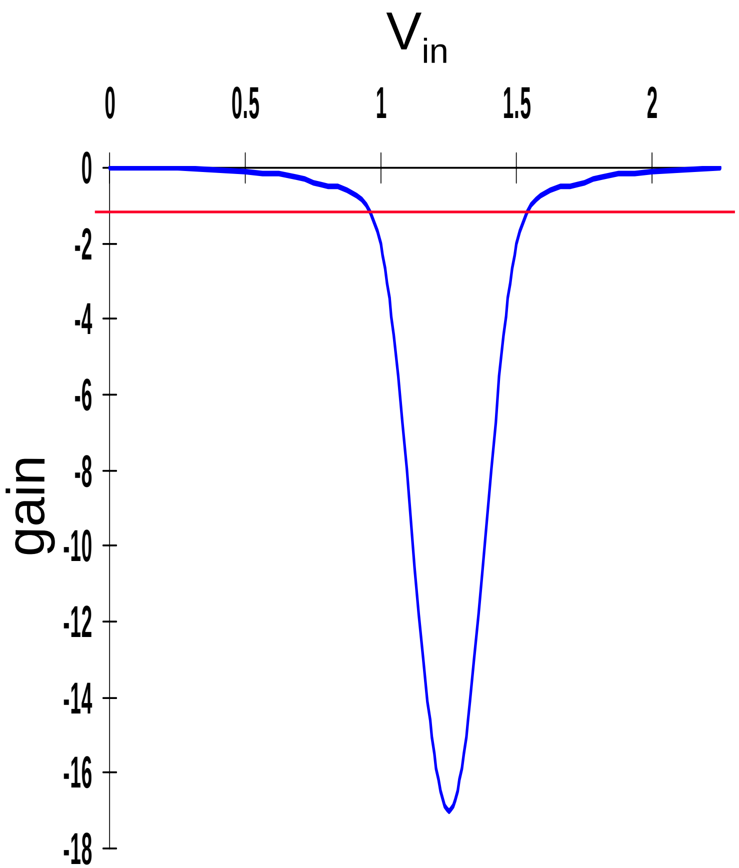
$NM_H = V_{DD} - V_{IH}$
$NM_L = V_{IL}$ - GND

Approximating:

$V_{IH} = V_M - V_M/g$
$V_{IL} = V_M + (V_{DD} - V_M)/g$

So high gain in the transition region is very desirable

Gain Determinates

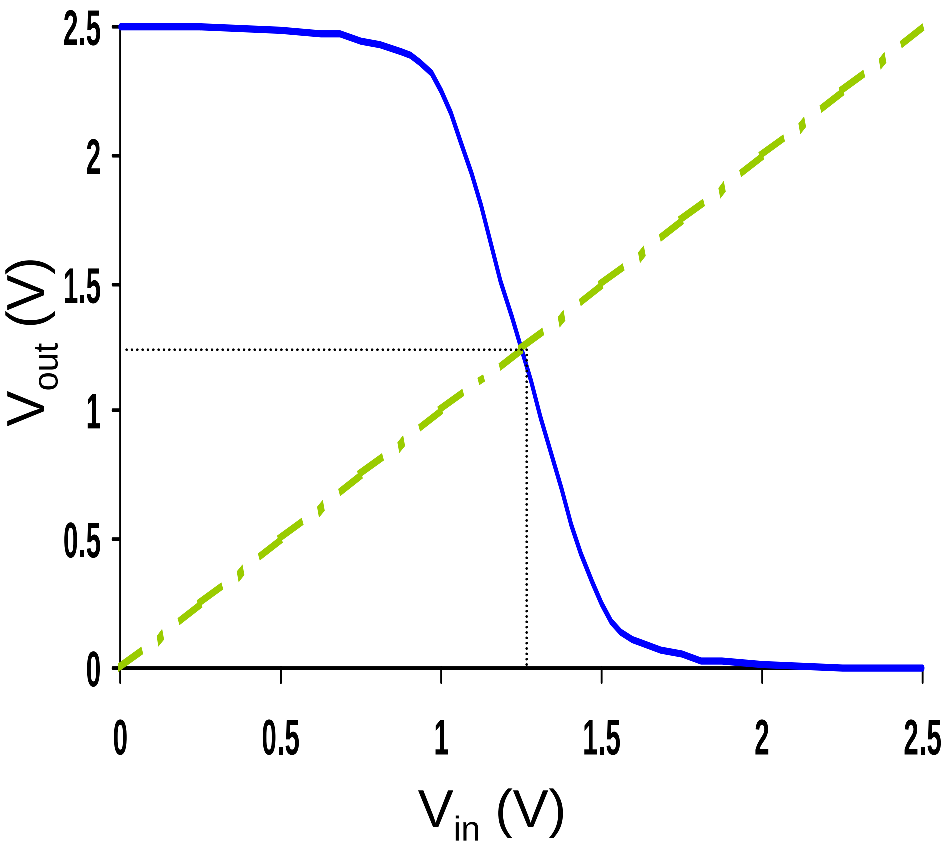


Gain is a strong function of the slopes of the currents in the saturation region, for $V_{in} = V_M$

$$g \approx \frac{(1+r)}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

Determined by technology parameters, especially channel length modulation (λ). Only designer influence through supply voltage and V_M (transistor sizing).

CMOS Inverter VTC from Simulation



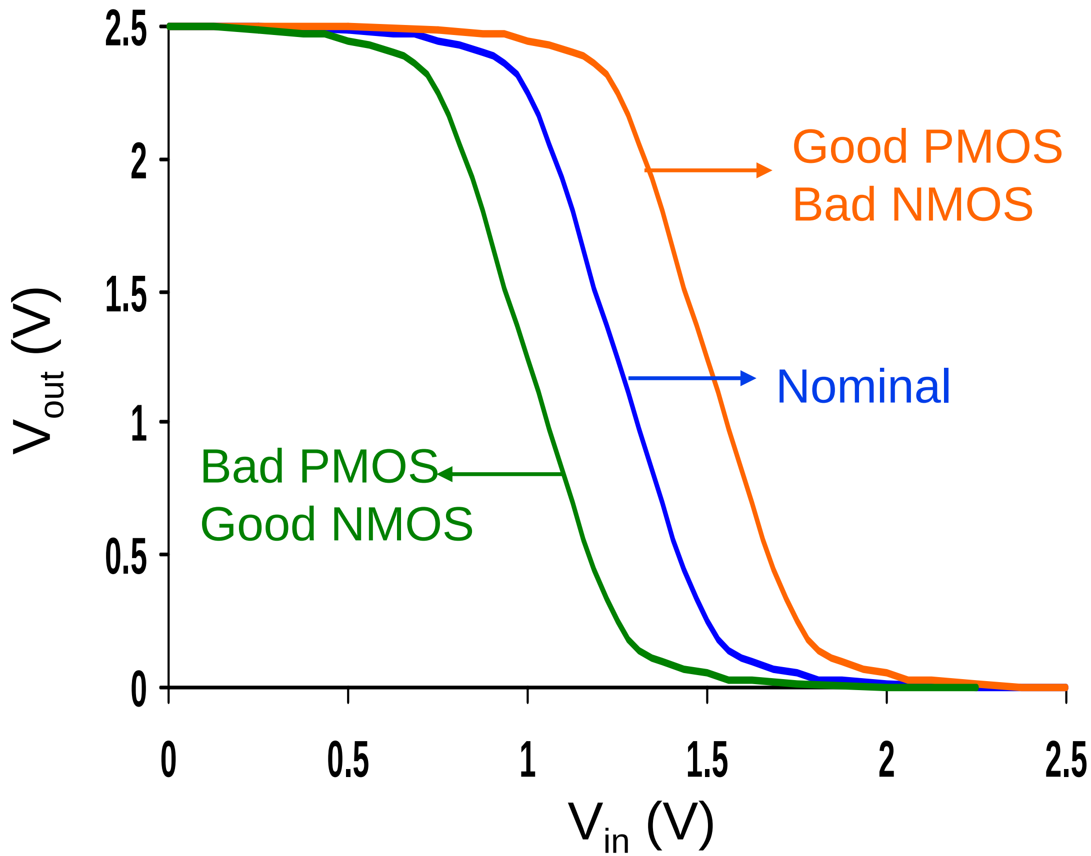
0.25um, $(W/L)_p/(W/L)_n = 3.4$
$(W/L)_n = 1.5$ (min size)
$V_{DD} = 2.5V$

$V_M \approx 1.25V$, g = -27.5

$V_{IL} = 1.2V$, $V_{IH} = 1.3V$
$NM_L = NM_H = 1.2$
(actual values are
$V_{IL} = 1.03V$, $V_{IH} = 1.45V$
$NM_L = 1.03V$ & $NM_H = 1.05V$)

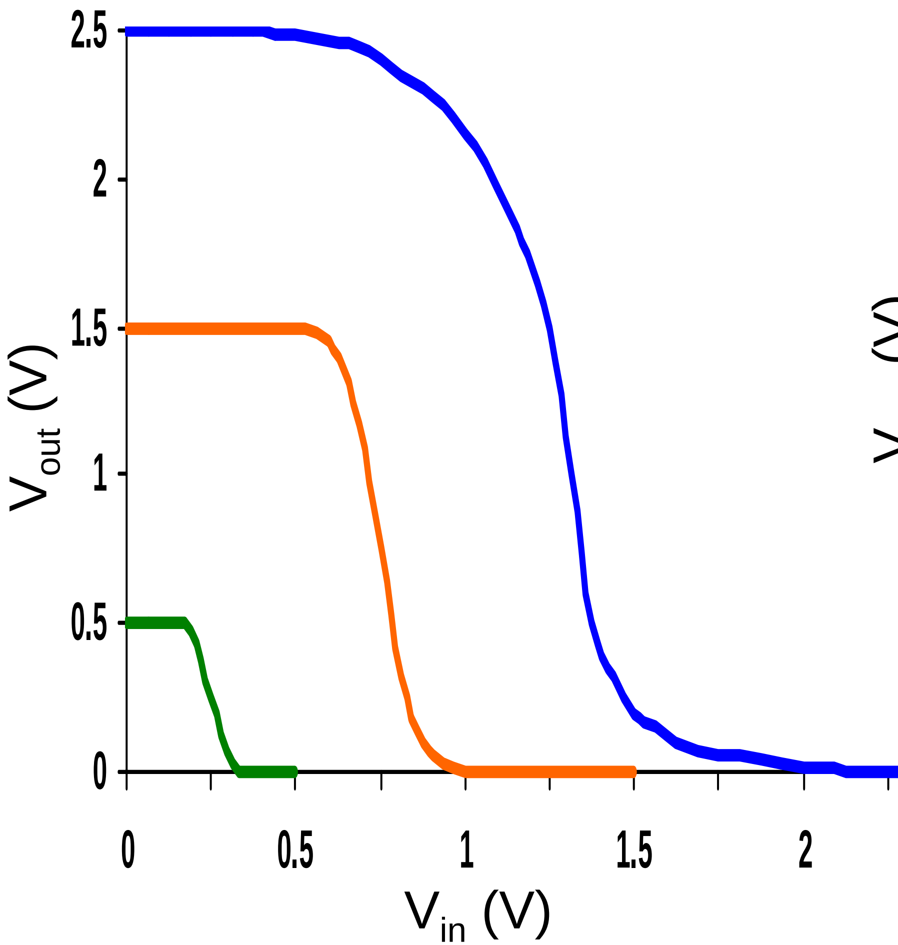
Output resistance
low-output = 2.4kΩ
high-output = 3.3kΩ

Impact of Process Variation on VTC Curve

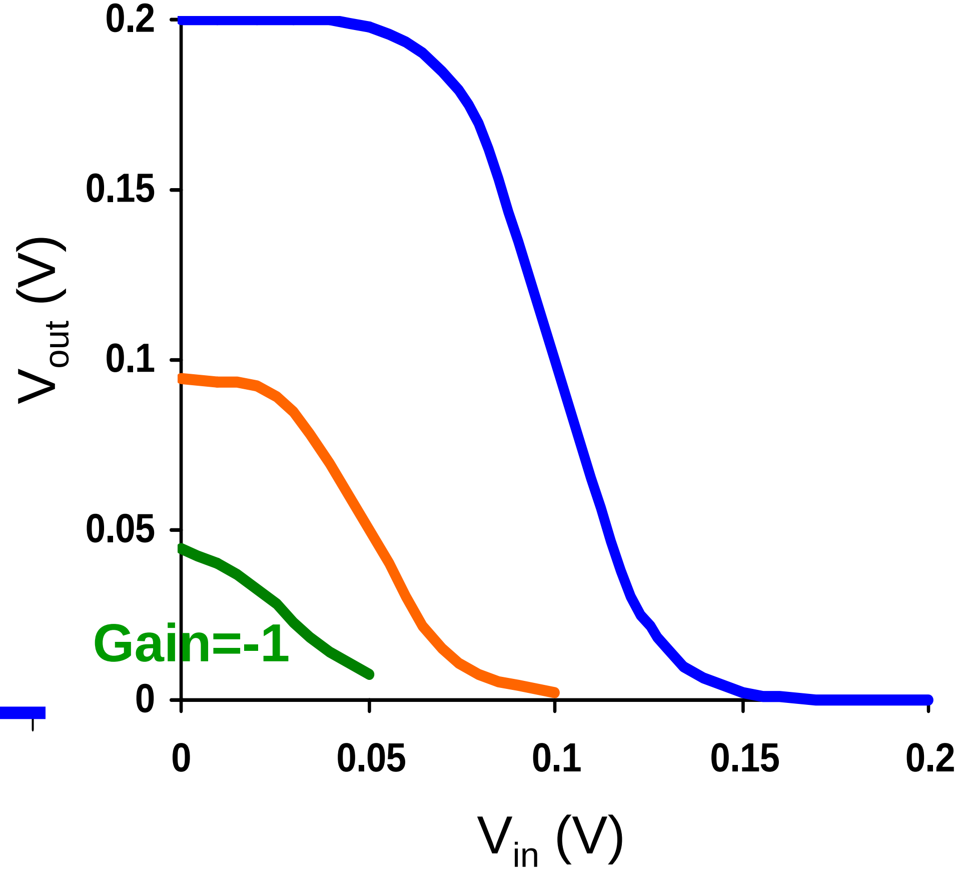


- Process variations (mostly) cause a shift in the switching threshold

Scaling the Supply Voltage



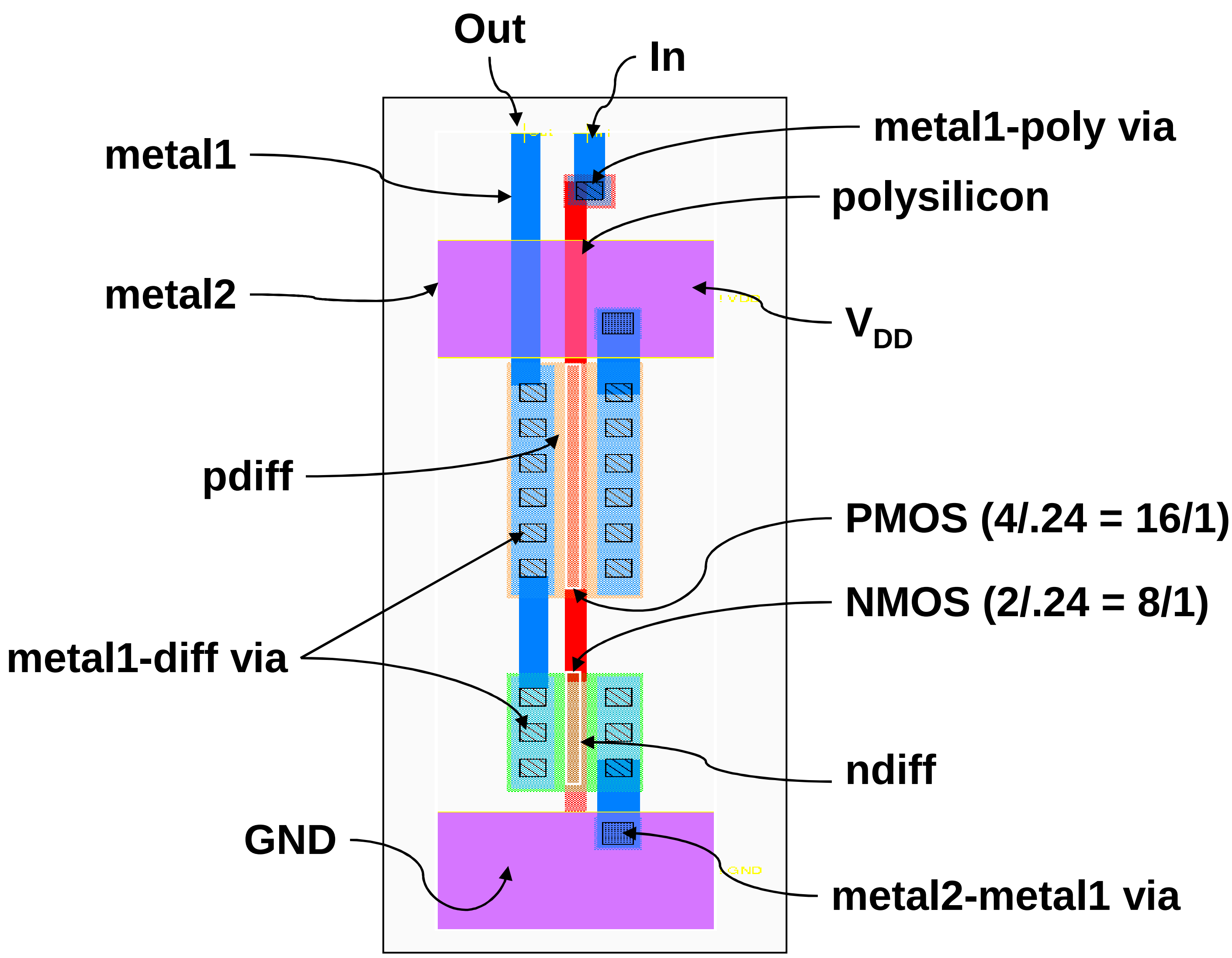
Device threshold voltages are kept (virtually) constant



Device threshold voltages are kept (virtually) constant

Project Partner

Next Time: CMOS Inverter *max* Layout



Next Lecture and Reminders

- Next lecture
  - IC manufacturing
    - Reading assignment – Rabaey, et al, 2.1-2.3

- Reminders
  - HW1 due today, HW2 is out and due on Feb 10
  - Project team and title due Jan 27 (next class!)