The Fundamentals of DS3

Overview

To meet the growing demands of voice and data communications, America's largest corporations are exploring the high-speed worlds of optical fiber and DS3 circuits. As end-users continue to demand more throughput, the move to DS3 circuits is often the best solution for DS1-based private networks. Today's DS3 tariff rates are designed to attract customers, even if these customers can't immediately take advantage of the extra bandwidth. And, depending on location and distance, a DS3 circuit will cost about the same amount as four to 10 DS1 circuits. Once the jump to DS3 bandwidth is made, users have a cost-effective means to implement a host of new communication technologies including video conferencing, workstation-based graphics, distributed data processing, and more advanced facsimile transmission.

Because of the increasing presence of DS3 circuits, understanding the DS3 channel is imperative. This ***Technical Note*** provides a detailed description of how the DS3 channel is formed or multiplexed from 28 separate DS1 channels. It is assumed that the reader has a basic understanding of the DS1 framing format.

The multiplexing involved in forming a DS3 signal is a two-step process. First, the 28 DS1 signals are multiplexed into seven separate DS2 signals, where each DS2 signal contains four DS1 signals. Second, the seven DS2 signals are combined to form the DS3 signal.

DS1 Framing Format Review

To review very briefly, the DS1 frame contains 24 8-bit DS0 channels and a framing bit for a total of 193 bits in the frame. Each 8-bit DS0 channel operates at a sampling rate of 8 kHz, which is also the DS1 frame rate. Therefore, the total aggregate bit rate for DS1 is:

193 bits/frame x 8,000 frame/sec = 1.544 Mb/s

which is the nominal bit rate for DS1.

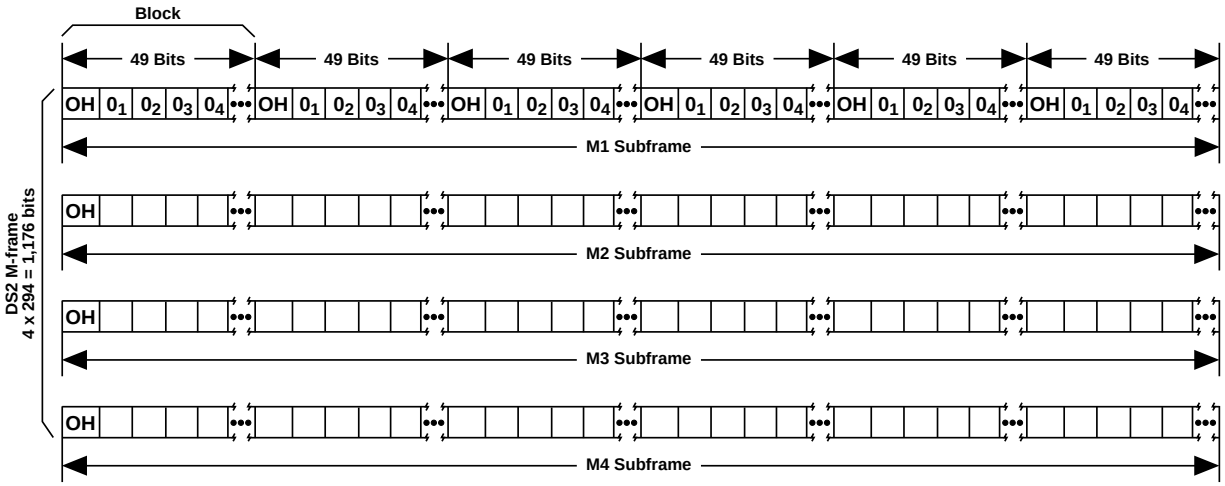
DS2 Framing Format

The first step in the two-step DS1-to-DS3 multiplexing process is to form a DS2 signal by combining four DS1 signals. ***Figure 1*** on the next page shows the DS2 framing format. The DS2 frame (sometimes called a DS2 M-frame) is composed of four subframes, designated M1 thru M4. Each subframe consists of six blocks and each block contains 49 bits. The first bit in each block is a DS2 overhead (OH) bit. Each DS2 frame contains 24 of these OH bits (1 OH bit/block x 6 blocks/subframe x 4 subframes/DS2 frame). The remaining 48 bits in a block are DS1 information bits. The total number of DS1 information bits in a DS2 frame is:

48 DS1 bits/block x 6 blocks/subframe x
4 subframes/DS2 frame = 1,152 DS1 information bits

The four subframes do *not* represent each of the separate DS1 signals. Rather, the DS2 frame is formed by bit-by-bit interleaving the four DS1 signals, as demonstrated in ***Figure 1***.

The OH bit leads off every block and is followed by the interleaved DS1 data bits where 0_i designates the time slot devoted to DS1 input i. After every 48 DS1



NOTES:

1. 0_i designates a time slot devoted to DS1 input i as part of the bit-by-bit interleaving process.
2. 6 blocks/M-subframe x 49 bits/block = 294 bits/M-subframe.

Figure 1
DS2 framing format.

information bits, 12 from each DS1 signal, a DS2 OH bit is inserted. The total number of DS1 information bits transmitted in one second in a DS2 frame is:

DS1 rate x 4 DS1 signals per DS2 which is
1.544 Mb/s x 4 DS1 signals/DS2 = 6.176 Mb/s

The overall rate chosen for DS2 is 6.312 Mb/s. The reason this rate is chosen is to provide extra bandwidth for DS2 bit stuffing and DS2 OH bits as explained below.

DS2 Bit Stuffing

The four DS1 signals are asynchronous relative to each other, and therefore may be operating at different rates. A synchronization method used by multiplexers, called bit stuffing (or pulse stuffing[1]), is used to adjust the different incoming rates. Bit stuffing is explained in greater detail in the Bit Stuffing sidebar on page 4.

DS2 OH Bits

The DS2 OH bits provide alignment and bit stuffing control. The OH bits are located in the first bit position of every block. ***Figure 2*** shows the location of the various DS2 overhead bits designated F, M, and C.

F-bits

The F-bits (framing bits) form the frame alignment signal. There are eight F-bits per DS2 frame (two

[1]Bell Laboratories, *Transmission Systems for Communications,* (Holmdel, N.J.: Bell Telephone Laboratories, Inc., 1982), pp. 675-680.

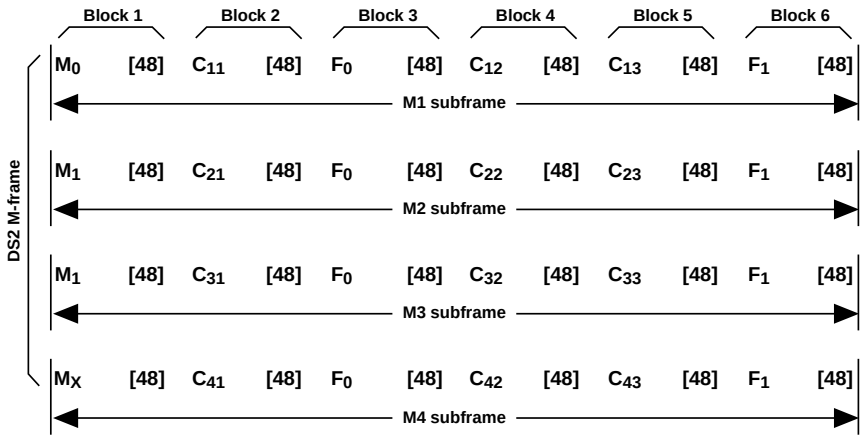


Figure 2
DS2 overhead bits.

Notes:

1. $F_0 F_1$ is the frame alignment signal. $F_0 = 0$ and $F_1 = 1$.
2. $M_0 M_1 M_1 M_X$ is the multiframe alignment signal. $M_0 = 0$, $M_1 = 1$, and M_X may be a 0 or a 1.
3. $C_{11} C_{12} C_{13}$ = stuffing indicators for DS1 input 1.
   $C_{21} C_{22} C_{23}$ = stuffing indicators for DS1 input 2.
   $C_{31} C_{32} C_{33}$ = stuffing indicators for DS1 input 3.
   $C_{41} C_{42} C_{43}$ = stuffing indicators for DS1 input 4.
   If the three C-bits in subframe i are all zeros, no stuffing was done for DS1 input i. If the three C-bits are all ones, stuffing was done.
4. [48] represents 48 DS1 information bits between every DS2 OH bit.

per subframe). The F-bits are located in the first bit position in blocks 3 and 6 of each subframe. The frame alignment pattern, which is repeated every subframe, is "01".

The rate of framing bit errors is a good in-service approximation of the logic bit error rate because of the number and location of framing bits.

M-bits

The M-bits (multiframing bits) form the multiframe alignment signal. There are four M-bits per DS2 frame (one per subframe). The M-bits are located in the first bit position in each subframe. Transmission equipment uses the M-bit pattern, "011X", (where X can be a "0" or a "1") to locate the four subframes.

C-bits

The C-bits are used to control bit stuffing. There are three C-bits per subframe, designated C_{ij} (see ***Figure 2***), where i corresponds to the subframe number and j refers to the position number of the C-bit in a particular subframe. Refer to Appendix A on page 10 for details on how the C-bits are used to control bit stuffing within the DS2 frame.

Bit Stuffing Basics

Bit stuffing is a synchronization method used by multiplexers to adjust for different incoming rates. Bit stuffing works by making the overall output rate high enough to handle a range of input rates. For example, four DS1 signals multiplexed into a DS2 signal require the following minimum bandwidth:

4 x 1.544 Mb/s (nominal DS1)	6,176,000 b/s
DS2 OH bits	+128,816 b/s
Total minimum DS2 bandwidth	6,304,816 b/s

The output rate normally chosen for DS2 is 6.312 Mb/s which is an even multiple of the 8 kHz sampling rate and provides extra bandwidth beyond the minimum requirement of 6,304,816 b/s. The extra bandwidth is used to accommodate bit stuffing for each incoming DS1 signal until each rate is increased to an "intermediate" rate of 1,545,796 b/s. Taking the sum of the four "intermediate" DS1 rates along with the DS2 OH bits gives the DS2 aggregate output rate of 6.312 Mb/s. During the multiplexing process the stuffed bits are inserted at fixed locations in the framing format, and are identified and removed during demultiplexing.

The output rate chosen for DS3 is 44.736 Mb/s which is also an even multiple of the 8 kHz sampling rate and provides the extra bandwidth necessary for bit stuffing at the DS3 level. Complete details on the mechanics of bit stuffing, for the standard M13 asynchronous format, at the DS2 and DS3 levels are provided in Appendices A and B, on pages 10 and 13, respectively. Appendix C on page 16 covers bit stuffing for the C-bit parity format.

DS3 Framing Format

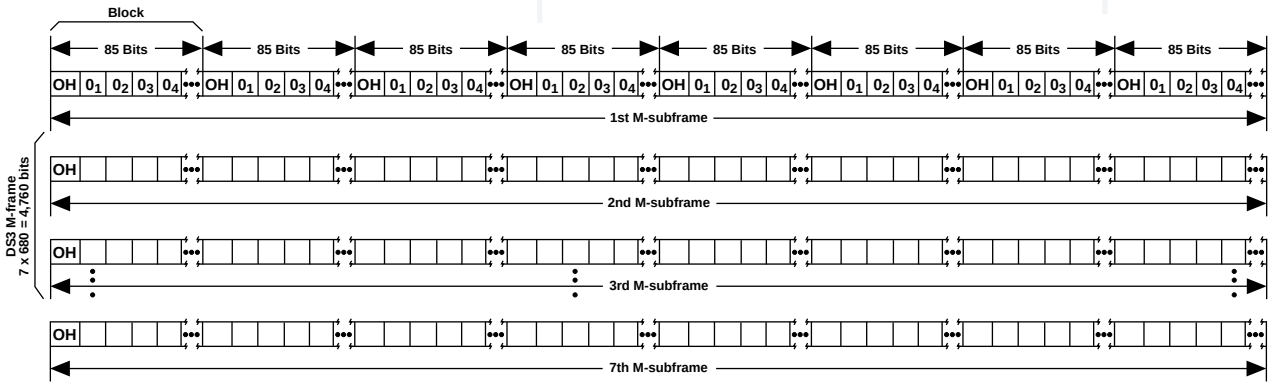
The second step in forming a DS3 signal is to multiplex seven DS2 signals (each containing four DS1 signals) into a DS3 signal. The same method that is used to multiplex the four DS1 signals into a DS2 signal applies. ***Figure 3*** shows the DS3 framing format, known as the standard M13 asynchronous format. M13 is the multiplex designation for multiplexing 28 DS1 signals into one DS3 signal. The DS3 frame (sometimes called a DS3 M-frame) is composed of seven subframes, designated 1st thru 7th. Each subframe consists of eight blocks and each block contains 85 bits. The first bit in each block is a DS3 OH bit. Each DS3 frame contains 56 of these OH bits (1 OH bit/block x 8 blocks/subframe x 7 subframes/DS3 frame). The remaining 84 bits in a block are DS2 information bits. The total number of DS2 information bits in a DS3 frame is:

84 DS2 bits/block x 8 blocks/subframe x
7 subframes/DS3 frame = 4,704 DS2 information bits

The seven subframes do *not* represent each of the separate DS2 signals. Instead, the DS3 frame is formed by bit-by-bit interleaving the seven DS2 signals, as demonstrated in ***Figure 3***. This interleaving process is the same as that used when the four DS1 signals are multiplexed together to form a DS2 signal. After every 84 DS2 information bits, 12 from each DS2 signal, a DS3 OH bit is inserted. The total number of DS2 information bits transmitted in one second is:

DS2 rate x 7 DS2 signals per DS3 which is
6.312 Mb/s x 7 DS2 signals = 44.184 Mb/s

The overall rate chosen for DS3 is 44.736 Mb/s. The reason this rate is chosen is to provide extra bandwidth for DS3 bit stuffing and DS3 OH bits as explained on the next page.



NOTES:

1. 0_i designates a time slot devoted to DS2 input i.
2. 8 blocks/M-subframe x 85 bits/block = 680 bits/M-subframe.

Figure 3
DS3 framing format.

DS3 Bit Stuffing

The seven DS2 signals may be asynchronous relative to each other (because they may not have been formed within a common multiplexer) and therefore may be operating at different rates. Bit stuffing, again, is used to adjust the different incoming rates. Bit stuffing is explained in greater detail in the Bit Stuffing sidebar.

DS3 OH Bits

The DS3 OH bits provide alignment, error checking, in-band communications, and bit stuffing control information. The OH bits are located in the first bit position of every block. ***Figure 4*** on the next page shows the location of the various DS3 OH bits.

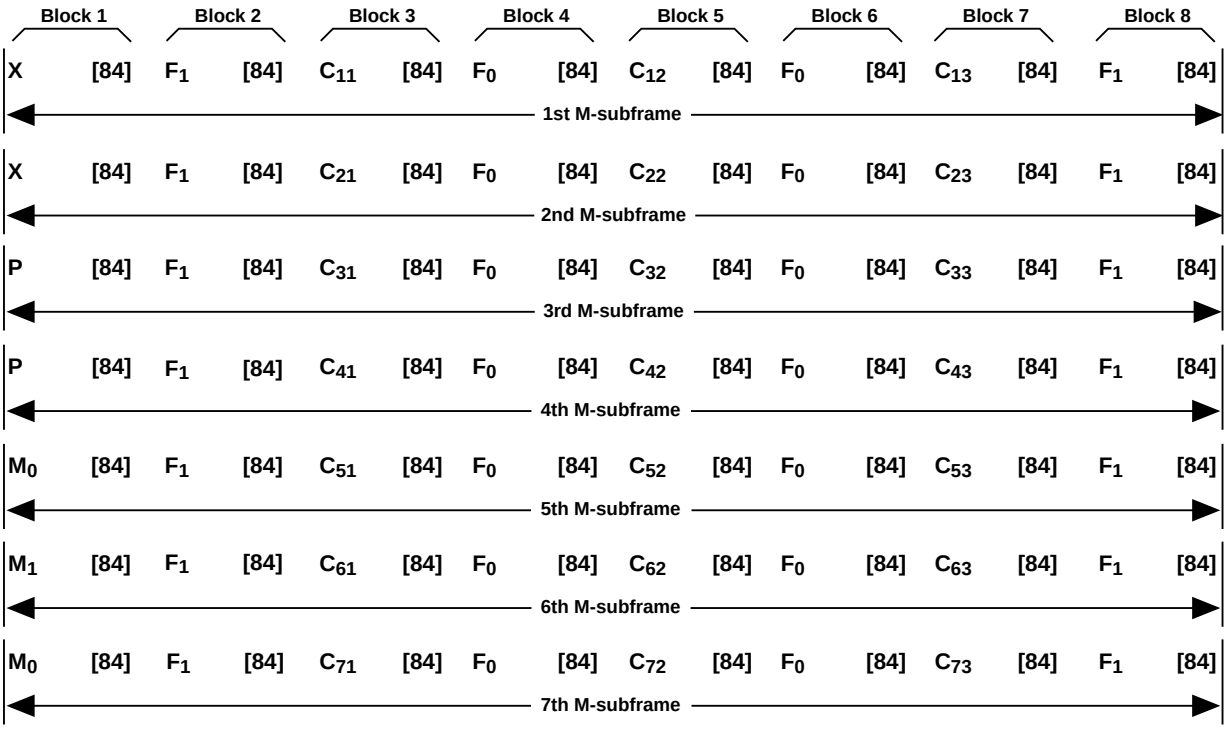
F-bits

The F-bits (framing bits) form the frame alignment signal. There are 28 F-bits per DS3 frame (four per subframe). The F-bits are located in the first bit position in blocks 2, 4, 6, and 8 of each subframe. The frame alignment pattern, which is repeated every subframe, is "1001".

The rate of framing bit errors is a good in-service approximation of the logic bit error rate because of the number and location of framing bits.

M-bits

The M-bits (multiframing bits) form the multiframe alignment signal. There are three M-bits per DS3 frame. The M-bits are located in the first bit position in block 1 of subframes 5, 6, and 7. DS3 equipment use the M-bit "010" pattern to locate the seven subframes.



NOTES:

1. $F_1 F_0 F_0 F_1$ is the frame alignment signal. $F_0 = 0$ and $F_1 = 1$.
2. $M_0 M_1 M_0$ is the multiframe alignment signal. $M_0 = 0$ and $M_1 = 1$.
3. P is the parity information taken over all information bits in the preceding M-frame. Both P-bits equal 1 if the digital sum of all information bits is 1. Both P-bits equal 0 if the sum is 0.
4. The X-bits may be used for the transmission of in-service meassages. In any one M-frame the two X-bits must be identical and may not change more than once per second.
5. $C_{11} C_{12} C_{13}$ = stuffing indicators for DS2 input 1.
   $C_{21} C_{22} C_{23}$ = stuffing indicators for DS2 input 2.
   $C_{31} C_{32} C_{33}$ = stuffing indicators for DS2 input 3.
   $C_{41} C_{42} C_{43}$ = stuffing indicators for DS2 input 4.
   $C_{51} C_{52} C_{53}$ = stuffing indicators for DS2 input 5.
   $C_{61} C_{62} C_{63}$ = stuffing indicators for DS2 input 6.
   $C_{71} C_{72} C_{73}$ = stuffing indicators for DS2 input 7.
   If the three C-bits in subframe i are all zeros, no stuffing was done for DS2 input i. If the three C-bits are all ones, stuffing was done.
6. [84] represents 84 DS2 information bits between every DS3 OH bit.

Figure 4
DS3 overhead bits.

C-bits

The C-bits are used to control bit stuffing. There are three C-bits per subframe, designated C_{ij} (see ***Figure 4***), where i corresponds to the subframe number and j refers to the position number of the C-bit in a particular subframe. Refer to Appendix B on page 13 for details on how the C-bits are used to control bit stuffing within the DS3 frame.

X-bits

The X-bits (message bits) may be used by a DS3 source for asynchronous in-service messages (i.e., the message is embedded in the data). There are two X-bits per DS3 frame. The X-bits are located in the first bit position in block 1 of subframe 1 and subframe 2. In any one DS3 frame the two X-bits must be identical, either both ones or both zeros. Also, the source may not change the state of the X-bits more than once every second.

P-bits

The P-bits (parity bits) contain parity information. There are two P-bits per DS3 frame. The P-bits are located in the first bit position in block 1 of subframe 3 and subframe 4. DS3 sources compute parity over all 4,704 DS3 information bits (4,760 total bits – 56 OH bits) following the first X-bit in a DS3 frame. The resulting parity information is inserted in the P-bit positions of the following frame. The state of the two P-bits within a single DS3 frame is always identical. The two P-bits are set to "1" if the previous DS3 frame contained an odd number of ones. Conversely, the two P-bits are set to "0" if the previous DS3 frame contained an even number of ones.

The parity bits provide a means of in-service error detection. If, on the receive-side, the number of ones for a given frame does not match the parity information in the following frame, one or more bit errors occurred during the transmission.

C-bit Parity Framing Format

The standard M13 asynchronous format uses all 21 DS3 C-bits for bit stuffing control. Since M13 multiplexers perform bit stuffing when forming the seven DS2 signals from the 28 DS1 signals, the resulting DS2 signals are synchronous to each other. Therefore, the bit stuffing which takes place when the seven DS2 signals are multiplexed into the single DS3 signal is a redundant process.

By redefining the two-step multiplexing method, this redundant bit stuffing process can be eliminated. This redefinition results in a new format, called DS3 C-bit parity. The C-bit parity format, unlike the M13 format, does not use the DS3-level C-bits for bit stuffing control. Instead, the C-bits, as well as the X-bits, are redefined, making it possible to provide (a) in-service, end-to-end path performance monitoring of the DS3 signal, and (b) in-band data links.

C-bit Parity Format OH Bits

Figure 5 on the next page shows the OH bits within the C-bit parity format. The definitions for the framing, multiframing, and parity bits are the same as the defintions within the standard M13 asynchronous format. The new X-bit and C-bit defintions are described below (as per the T1X1.4 Working Group):

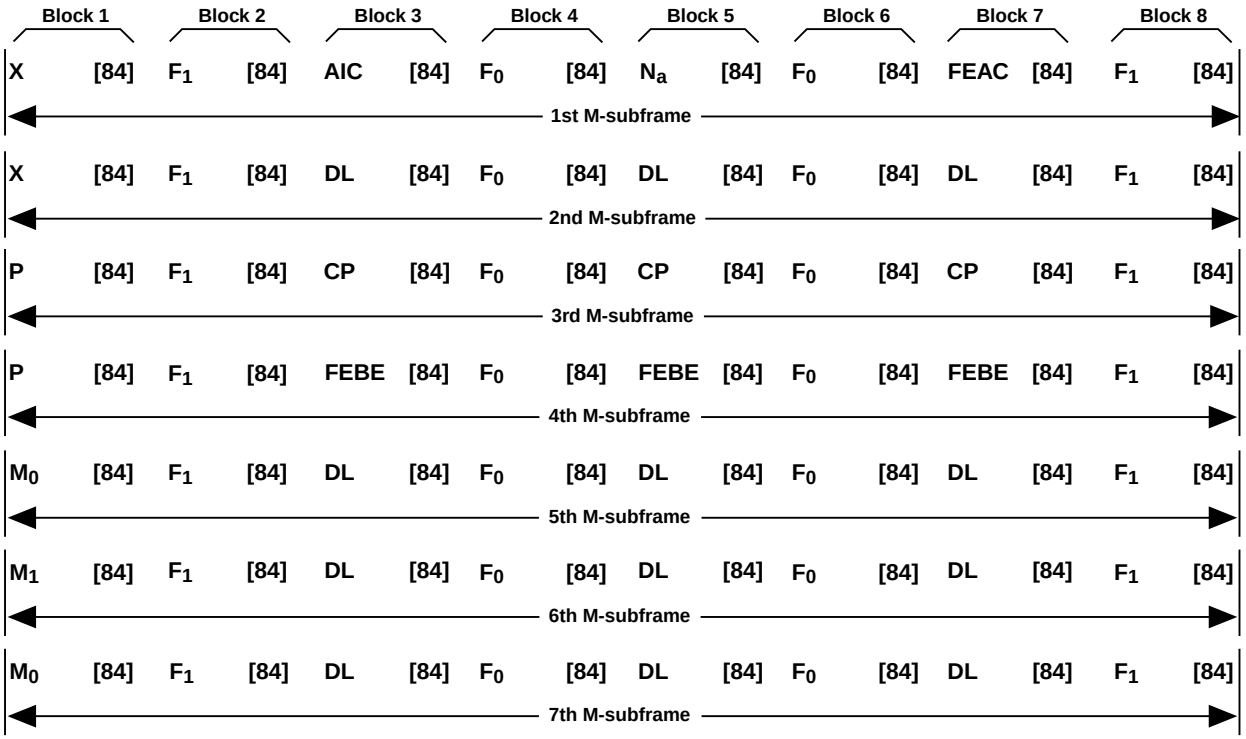
X-bits

In C-bit parity the X-bits are used to transmit what is termed a "degraded second" from the far-end of the system to the near-end of the system by modulating the X-bits at no more than a one-second rate. That is, at the far-end terminal, if an incoming out-of-frame or alarm indication signal (AIS) condition is detected anytime during a one-second interval, that condition is transmitted to the near-end terminal where it will be detected as a degraded second. This is done by setting both X-bits in the outgoing direction to "0" for one second; otherwise both X-bits are set to "1".

C-bits

Application Identification Channel (AIC)

The first C-bit in subframe 1 is defined as an AIC and can be used by DS3 terminal equipment (TE) to automatically identify a specific DS3 framing format. For C-bit parity, this position is set to a "1".



NOTES:

1. $F_1 F_0 F_0 F_1$ is the frame alignment signal. $F_0 = 0$ and $F_1 = 1$.
2. $M_0 M_1 M_0$ is the multiframe alignment signal. $M_0 = 0$ and $M_1 = 1$.
3. P is the parity information taken over all information bits in the preceding M-frame. Both P-bits equal 1 if the digital sum of all information bits is 1. Both P-bits equal 0 if the sum is 0.
4. The X-bits are used to transmit a "degraded second" from the far-end to the near-end. In any one M-frame the two X-bits must be identical and may not change more than once per second.
5. C-bit definitions:
   AIC = Application Identification Channel = 1.
   N_a = Reserved Network Application Bit..
   FEAC = Far-End Alarm and Control Channel.
   DL = Data Link.
   CP = C-bit Parity.
   FEBE = Far-End Block Error.
6. [84] represents 84 DS2 information bits between every DS3 OH bit.

Figure 5
C-bit parity overhead bits.

Reserved Network Application Bit

The second C-bit in subframe 1, designated N_a, is reserved for future applications.

Far-End Alarm and Control (FEAC) Channel

The third C-bit in subframe 1 is used as a FEAC channel, where alarm or status information from the far-end terminal can be sent back to the near-end terminal.

This channel is also used to initiate DS3 and DS1 line loopbacks at the far-end terminal from the near-end terminal. A simple, repeating, 16-bit code word, of the form

0XXXXXX011111111 where "X" can be a "0" or a "1"

with the rightmost bit transmitted first, can be used to indicate one of several possible alarm or status conditions. When no alarm or status condition is being transmitted, the FEAC channel is set to all ones. Refer to the latest document issued by the T1X1.4 Working Group for a complete listing of the FEAC code words.

Data Links (DL)

The 12 C-bits located in subframes 2, 5, 6, and 7, all designated DL, are defined as data links for applications and terminal-to-terminal path maintenance. Refer to the latest document issued by the T1X1.4 Working Group for a complete description of how these bits are used.

DS3 Path Parity Bits

The three C-bits in subframe 3, designated CP-bits, are used to carry the DS3 path parity information. At the DS3 TE transmitter the CP-bits are set to the same value as the two P-bits. Since the CP-bits will pass through the network unchanged (except in the case of errors), the DS3 TE receiver can determine if an error occured in an M-frame by computing the parity based on the contents of the given M-frame and comparing this parity value with the parity received in the CP-bits in the following M-frame.

NOTE: The normal P-bits cannot provide DS3 path monitoring because they are subject to correction by each facility section the the DS3 path. Therefore, the M13 format cannot provide end-to-end path parity information. The C-bit parity format has a big advantage over the M13 format by providing end-to-end parity checking.

Far-End Block Error (FEBE) Function

The FEBE function uses the three C-bits in subframe 4 and can best be understood as illustrated in the following example. Refer to ***Figure 6.*** The near-end TE monitors its incoming direction of transmission (west-bound) for the occurrence of a framing or parity error event. Upon detecting a framing or parity error event via the west-bound CP-bits, the near-end TE will (a) count the event as a C-bit parity error, and (b) indicate to the far-end TE the occurrence of the error via the east-bound FEBE bits by setting the three FEBE bits to "000" to indicate the error. (The three FEBE bits are set to "111" if no parity error event occurred.) Since DS3 TE monitors both the CP and FEBE bits, as well as the FEAC channel, the overall performance of the DS3 path, for both directions of transmission, can be determined at either end of the path.

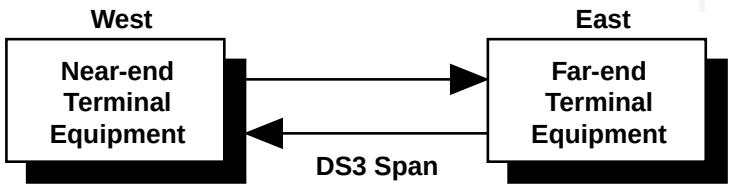


Figure 6
DS3 span.

Summary

The DS3 signal is composed of 28 DS1 signals and is constructed using a two-step multiplexing process. First, the 28 DS1 signals are multiplexed into seven DS2 signals. Second, the seven DS2 signals are multiplexed into one DS3 signal. Each multiplexing step uses bit stuffing to handle the different input frequencies. OH bits provide alignment, error checking, in-band communications, and bit stuffing control information.

The standard M13 format used widely today cannot provide end-to-end path parity information; a maintenance feature which is becoming more important as DS3 circuits become more prevalent. The C-bit parity format redefines the use of the C-bits in the M13 frame making it possible to provide in-service, end-to-end path performance monitoring of the DS3 signal and in-band data links. The ability to monitor degraded seconds, bidirectional end-to-end parity, and far-end alarms gives the C-bit parity format additional maintenance functionality over the M13 format.

Appendix A: The Mechanics of Bit Stuffing within the DS2 Frame

The DS2 C-bits are used as bit stuffing indicators during the first step of DS1-to-DS3 multiplexing: combining four DS1 signals into a single DS2 signal. There are three C-bits per DS2 subframe, designated C_{ij} (see ***Figure 2***), where i corresponds to the subframe number and j refers to the position number of the C-bit in a particular subframe.

In each DS2 frame one bit can be stuffed for each of the four DS1 signals. Specifically, the state of the three C-bits in the i^{th} subframe indicates whether or not bit stuffing occurs for the i^{th} DS1 input during the multiplexing process. The state of the C-bits is physically determined by the multiplexing equipment. If the three C-bits are all ones, stuffing occurs. The location if the stuffed bit is the first information bit position (designated 0_i) associated with the i^{th} DS1 signal following the last F_1 bit in a subframe. If the three C-bits are all zeros, no stuffing occurs and the associated "stuffable" bit position is merely treated as normal DS1 data bit.

During the demultiplexing process, the C-bits are used to determine if the "stuffable" bit is to be included in the reconstructed DS1 signal. For example, if $C_{21}=C_{22}=C_{23}=0$ then bit 0_2 following F_1 in the M2 subframe is a data bit and therefore is included in the reconstruction of the second DS1 signal. If $C_{21}=C_{22}=C_{23}=1$ then bit 0_2 following F_1 in the M2 subframe is a stuff bit and therefore is not included in the reconstruction of the second DS1 signal.

The purpose of using three C-bits instead of one is to minimize the chance of misidentifying the stuffing process if one of the C-bits is in error. Therefore, in actual practice, a majority vote of the three C-bits is used to more accurately control the stuffing process.

The ability to handle different DS1 signal rates can be calculated from the DS2 framing format. Since each DS2 frame allows for the stuffing of one bit for each of the four DS1 signals, the maximum stuffing rate for each DS1 signal is equal to the DS2 frame rate. A DS2 frame contains 1,176 bits as shown in ***Figure 1.*** Therefore the frame rate is:

6,312,000 b/s ÷ 1,176 bits/frame =
5,367.35 frames/sec

and the number of OH bits per second is:

5,367.35 frames/sec x 24 OH bits/frame =
128,816.40 OH b/s

The minimum stuffing rate is 0 b/s. The actual bit stuffing rate depends on the rate of the DS1 signal. The bit stuffing rate for a DS1 signal operating at the nominal rate is calculated as follows:

Total DS2 bits	6,312,000 b/s
Four DS1 signals (4 x 1.544 Mb/s)	-6,176,000 b/s
DS2 OH bits	-128,816 b/s
Stuffing bits available	7,184 b/s

These 7,184 bits are the total bits available for stuffing and are divided evenly over the four DS1 signals. Therefore, the bit stuffing rate for a DS1 signal operating at the nominal rate is:

7,184 b/s ÷ 4 DS1 signals = 1,796 b/s

The maximum allowable DS1 rate is computed as follows:

DS2 signal rate	6,312,000 b/s
DS2 OH bits	-128,816 b/s
Total DS1 bits	6,183,184 b/s

The total number of DS1 bits is allocated evenly across the four DS1 signals:

6,183,184 b/s ÷ 4 DS1 signals = 1,545,796 b/s

Therefore each DS1 signal may be input at a maximum rate of 1,545,796 b/s. The bit stuffing rate for a DS1 signal operating at this rate is 0 b/s.

The minimum allowable DS1 rate is computed by taking the maximum allowable DS1 rate and subtracting the maximum stuffing rate (i.e., the DS2 frame rate) as follows:

Maximum DS1 rate	1,545,796 b/s
Maximum stuff rate	-5,367 b/s
Minimum DS1 rate	1,540,429 b/s

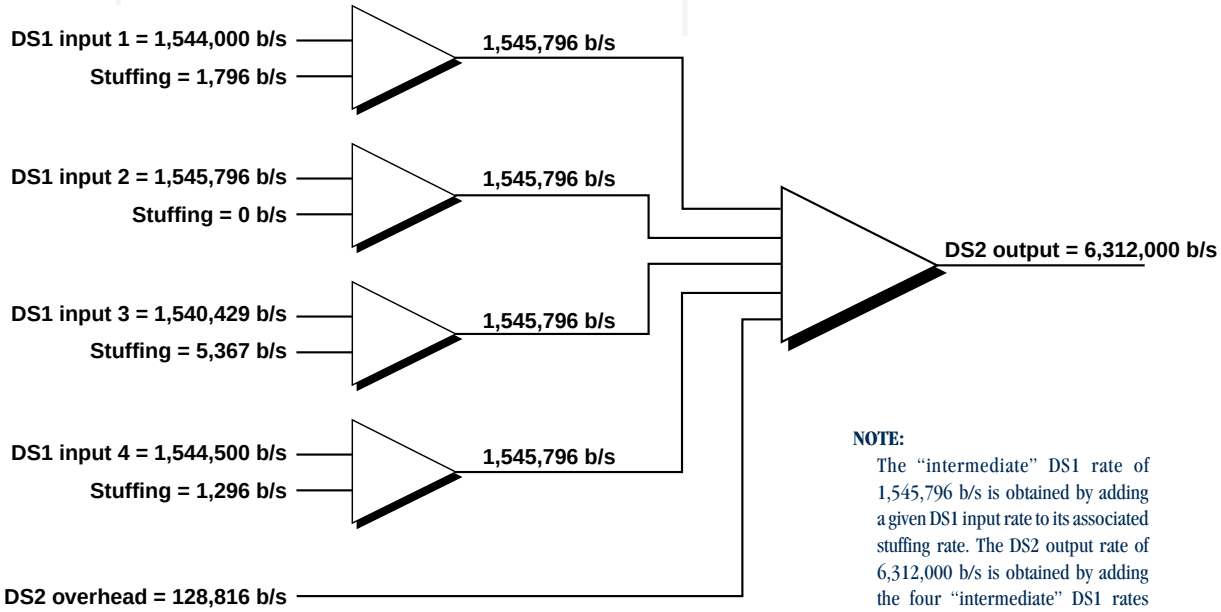
Therefore each DS1 signal may be input at a minimum rate of 1,540,429 b/s. The bit stuffing rate for a DS1 signal operating at this rate is 5,367 b/s.

Figure 7 on the next page depicts a summary representation of the first step of DS1-to-DS3 M13-type multiplexing: combining four DS1 signals all operating at different rates. The DS1 input rates shown in ***Figure 7*** were chosen to demonstrate how the stuffing rates vary with different input rates. The DS2 output rate is the sum of all the following:

DS1 signal 1	1,544,000 b/s (nom)
DS1 signal 1 stuff rate	1,796 b/s
DS1 signal 2	1,545,796 b/s (max)
DS1 signal 2 stuff rate	0 b/s
DS1 signal 3	1,540,429 b/s (min)
DS1 signal 3 stuff rate	5,367 b/s
DS1 signal 4	1,544,500 b/s (ex)
DS1 signal 4 stuff rate	1,296 b/s
DS2 OH bits	128,816 b/s
DS2 output rate	6,312,000 b/s

NOTE:

1. The higher the DS1 rate the lower the associated bit stuffing rate because the sum of the two always totals to an "intermediate" DS1 rate of 1,545,796 b/s.
2. The bit stuffing rate for a DS1 signal operating at the nominal rate of 1,544,000 b/s is 1,796 b/s.
3. The bit stuffing rate for a DS1 signal operating at the maximum rate of 1,545,796 b/s is 0 b/s.
4. The bit stuffing rate for a DS1 signal operating at the minimum rate of 1,540,429 b/s is 5,367 b/s.
5. The "intermediate" DS1 rate after bit stuffing is 1,545,796 b/s (e.g., 1,544,000 b/s + 1,796 b/s) and is equal to the maximum DS1 input rate which can be tolerated.



NOTE:
The "intermediate" DS1 rate of 1,545,796 b/s is obtained by adding a given DS1 input rate to its associated stuffing rate. The DS2 output rate of 6,312,000 b/s is obtained by adding the four "intermediate" DS1 rates and the DS2 OH rates.

Figure 7
M13-type multiplexing of four DS1 signals.

Figure 8 shows how the minimum and maximum allowable DS1 rates fit into the typical operating mode of most DS1 communication systems. For M13-type multiplexing, the DS2 signal accepts DS1 input rates between 1,540,429 b/s and 1,545,796 b/s. This wide range of rates allows DS2 signals the flexibility to transmit proprietary encoded DS1 signals as well as the commonly used, framed 1,544,000 b/s ±50 b/s signal.

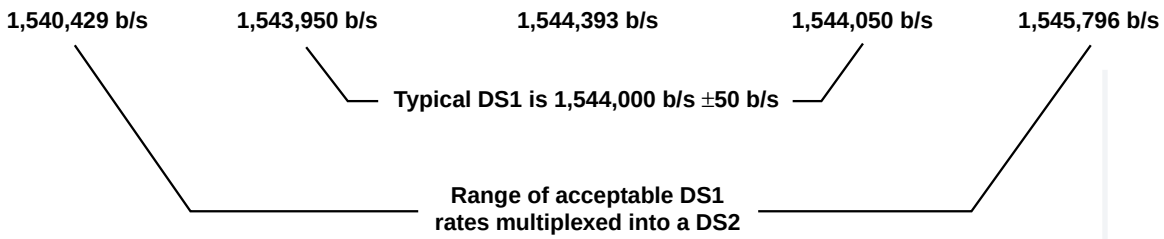


Figure 8
Range of DS1 rates.

Appendix B: The Mechanics of Bit Stuffing within the DS3 Frame

The DS3 C-bits are used as bit stuffing indicators during the second step of DS1-to-DS3 multiplexing: combining seven DS2 signals into a single DS3 signal. There are three C-bits per DS3 subframe, designated C_{ij} (see ***Figure 4***), where i corresponds to the subframe number and j refers to the position number of the C-bit in a particular subframe.

In each DS3 frame one bit can be stuffed for each of the seven DS2 signals. Specifically, the state of the three C-bits in the i^{th} subframe indicates whether or not bit stuffing occurs for the i^{th} DS2 input during the multiplexing process. The state of the C-bits is physically determined by the multiplexing equipment. If the three C-bits are all ones, stuffing occurs. The location of the stuffed bit is the first information bit position (designated 0_i) associated with the i^{th} DS2 signal following the last F_1 bit in a subframe. If the three C-bits are all zeros, no stuffing occurs and the associated "stuffable" bit position is merely treated as normal DS2 data bit.

During the demultiplexing process, the C-bits are used to determine if the "stuffable" bit is to be included in the reconstructed DS2 signal. For example, if $C_{61}=C_{62}=C_{63}=0$ then bit 0_6 following F_1 in the sixth M-subframe is a data bit and therefore is included in the reconstruction of the sixth DS2 signal. If $C_{61}=C_{62}=C_{63}=1$ then bit 0_6 following F_1 in the sixth M-subframe is a stuff bit and therefore is not included in the reconstruction of the sixth DS2 signal.

The purpose of using three C-bits instead of one is to minimize the chance of misidentifying the stuffing process if one of the C-bits is in error. Therefore, in actual practice, a majority vote of the three C-bits is used to more accurately control the stuffing process.

The ability to handle different DS2 signal rates can be calculated from the DS3 framing format. Since each DS3 frame allows for the stuffing of one bit for each

of the seven DS2 signals, the maximum stuffing rate for each DS2 signal is equal to the DS3 frame rate. A DS3 frame contains 4,760 bits as shown in ***Figure 3.*** Therefore the frame rate is:

44,736,000 b/s ÷ 4,760 bits/frame =
9,398.32 frames/sec

and the number of OH bits per second is:

9,398.32 frames/sec x 56 OH bits/frame =
526,305.92 OH b/s

The minimum stuffing rate is 0 b/s. The actual bit stuffing rate depends on the rate of the DS2 signal. The bit stuffing rate (for the M13 format) for a DS2 signal operating at the nominal rate is calculated as follows:

Total DS3 bits	44,736,000 b/s
Seven DS2 signals (7 x 6.312 Mb/s)	-44,184,000 b/s
DS3 OH bits	-526,306 b/s
Stuffing bits available	25,694 b/s

These 25,694 bits are the total bits available for stuffing and are divided evenly over the seven DS2 signals. Therefore the bit stuffing rate for a DS2 signal operating at the nominal rate is:

25,694 b/s ÷ 7 DS2 signals = 3,671 b/s

The maximum allowable DS2 rate is computed as follows:

DS3 signal rate	44,736,000 b/s
DS3 OH bits	-526,306 b/s
Total DS2 bits	44,209,694 b/s

The total number of DS2 bits is allocated evenly across the seven DS2 signals:

44,209,694 b/s ÷ 7 DS2 signals = 6,315,671 b/s

Therefore each DS2 signal may be input at a maximum rate of 6,315,671 b/s. The bit stuffing rate (for the M13 format) for a DS2 signal operating at this rate is 0 b/s.

The minimum allowable DS2 rate is computed by taking the maximum allowable DS2 rate and subtracting the maximum stuffing rate (i.e., the DS3 frame rate) as follows:

Maximum DS2 rate	6,315,671 b/s
Maximum stuff rate	-9,398 b/s
Minimum DS2 rate	6,306,272 b/s

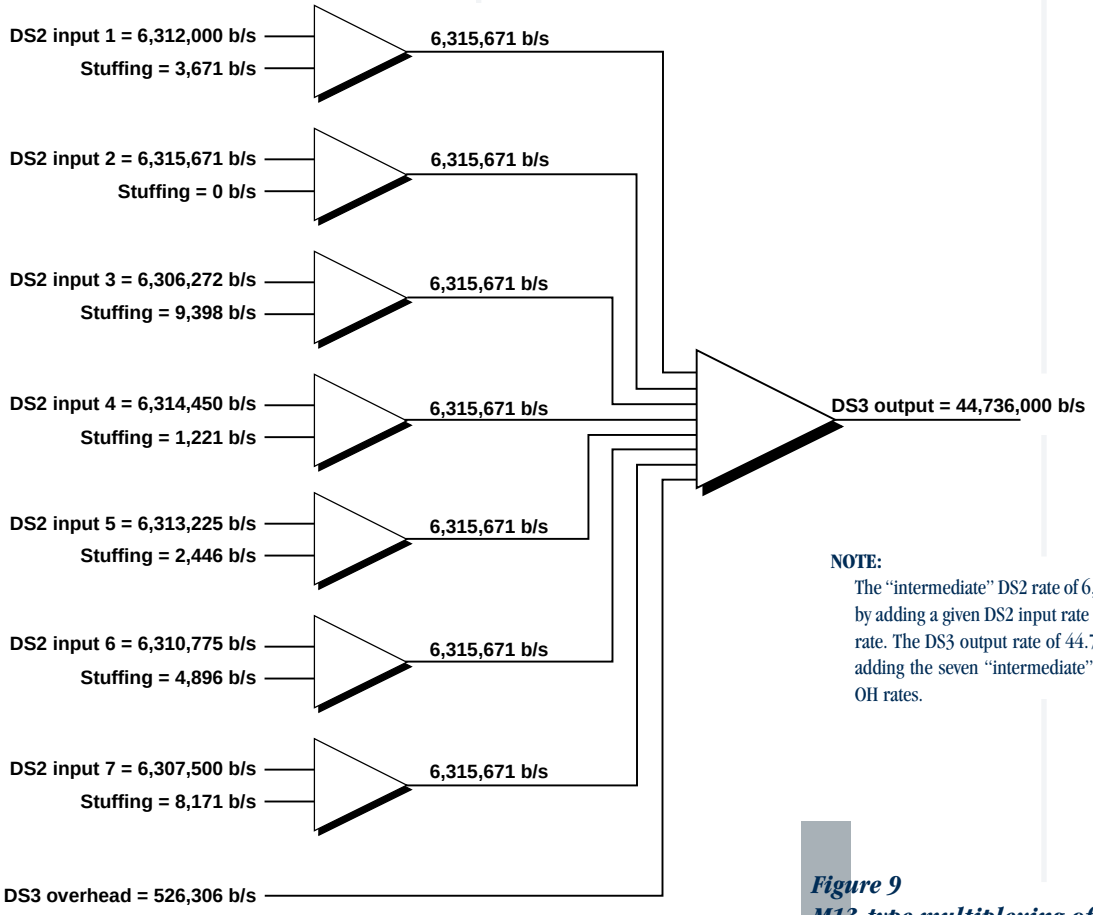
Therefore each DS2 signal may be input at a minimum rate of 6,306,272 b/s. The bit stuffing rate (for the M13 format) for a DS2 signal operating at this rate is 9,398 b/s.

Figure 9 depicts a summary representation of the second step of DS1-to-DS3 M13-type multiplexing: combining seven DS2 signals all operating at different rates. The DS2 input rates shown in ***Figure 9*** were chosen to demonstrate how the stuffing rates vary with different input rates. The DS3 output rate is the sum of all the following:

DS2 signal 1	6,312,000 b/s (nom)
DS2 signal 1 stuff rate	3,671 b/s
DS2 signal 2	6,315,671 b/s (max)
DS2 signal 2 stuff rate	0 b/s
DS2 signal 3	6,306,272 b/s (min)
DS2 signal 3 stuff rate	9,398 b/s
DS2 signal 4	6,314,450 b/s (ex)
DS2 signal 4 stuff rate	1,221 b/s
DS2 signal 5	6,313,225 b/s (ex)
DS2 signal 5 stuff rate	2,446 b/s
DS2 signal 6	6,310,775 b/s (ex)
DS2 signal 6 stuff rate	4,896 b/s
DS2 signal 7	6,307,500 b/s (ex)
DS2 signal 7 stuff rate	8,171 b/s
DS3 OH bits	526,306 b/s
DS3 output rate	44,736,000 b/s

NOTE:

1. The numbers do not add up exactly due to rounding off of the input frequencies.
2. The higher the DS2 rate the lower the associated bit stuffing rate because the sum of the two always totals to an "intermediate" DS2 rate of 6,315,671 b/s.
3. The bit stuffing rate for a DS2 signal operating at the nominal rate of 6,312,000 b/s is 3,671 b/s.
4. The bit stuffing rate for a DS2 signal operating at the maximum rate of 6,315,671 b/s is 0 b/s.
5. The bit stuffing rate for a DS2 signal operating at the minimum rate of 6,306,272 b/s is 9,398 b/s.
6. The "intermediate" DS2 rate after bit stuffing is 6,315,671 b/s (e.g., 6,312,000 b/s + 3,671 b/s) and is equal to the maximum DS2 input rate which can be tolerated.



NOTE:

The "intermediate" DS2 rate of 6,315,671 b/s is obtained by adding a given DS2 input rate to its associated stuffing rate. The DS3 output rate of 44.736 Mb/s is obtained by adding the seven "intermediate" DS2 rates and the DS3 OH rates.

Figure 9
M13-type multiplexing of seven DS2 signals into a DS3 signal.

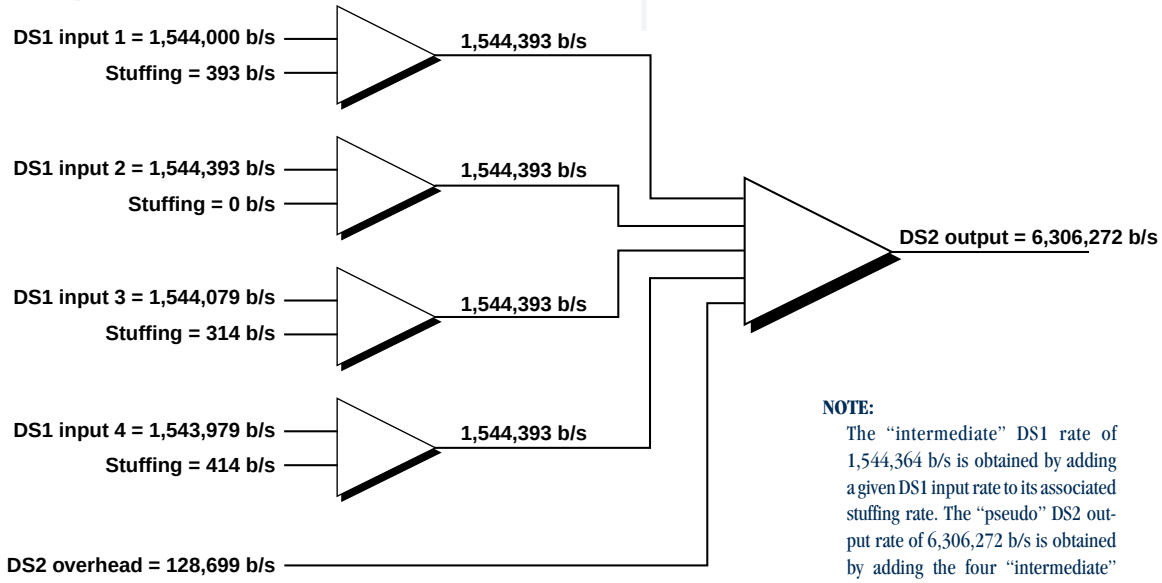
Appendix C: Bit Stuffing for the C-bit Parity Format

The reader should have a good understanding of Appendices A and B before reading Appendix C.

DS1-to-DS3 multiplexing using the C-bit parity format is the same two-step multiplexing process defined for the standard M13 asynchronous format except that bit stuffing is done at every opportunity during the second step of multiplexing. Since stuffing occurs 100% of the time, the C-bits are no longer needed for bit stuffing control. However, this "full-time" bit stuffing at the DS3 level requires the seven DS2 signals to be lower in frequency than the 6.312 Mb/s used with the standard M13 asynchronous format. Therefore, in the first step of multiplexing, four DS1 signals are multiplexed together to form a "pseudo" DS2 signal at a frequency of 6,306,272 b/s. This frequency is chosen such that the seven "pseudo" DS2 signals are multiplexed, along with the "full-time" DS3-level stuff bits and the 56 OH bits, to give the nominal DS3 output frequency of 44.736 Mb/s.

Figure 10 depicts a summary representation of the first step of DS1-to-DS3 C-bit parity-type multiplexing.

NOTE: The bit stuffing rates are lower than those used for the M13-type multiplexing ***(Figure 7)*** to yield an "intermediate" DS1 rate of 1,544,393 b/s (instead of 1,545,796 b/s) and hence a DS2 "pseudo" output rate of 6,306,272 b/s (instead of 6,312,000 b/s). This new "intermediate" DS1 rate forces the maximum allowable DS1 input rate (i.e., when bit stuffing is 0 b/s) to be 1,544,393 b/s.



NOTE:
The "intermediate" DS1 rate of 1,544,364 b/s is obtained by adding a given DS1 input rate to its associated stuffing rate. The "pseudo" DS2 output rate of 6,306,272 b/s is obtained by adding the four "intermediate" DS1 rates and the DS2 OH rates.

Figure 10
C-bit parity-type multiplexing of four DS1 signals.

If the multiplexing process shown in ***Figure 9*** were being done for the C-bit parity format instead of the standard M13 asynchronous format, the following would apply:

1. All the DS2 input rates would be at the "pseudo" frequency of 6,306,272 b/s (instead of 6,312,000 b/s).
2. All the stuffing rates would be at 9,398 b/s, the maximum stuffing rate.
3. The "intermediate" DS2 rate after bit stuffing would still be 6,315,671 b/s (6,306,272 b/s + 9,398 b/s).

Figure 11 shows the complete progression from a nominal DS1 rate (1.544 Mb/s) to a nominal DS3 rate (44.736 Mb/s) for both the standard M13 asynchronous format and the C-bit parity format.

	M13 Format	C-bit Format
Nominal DS1 rate	1,544,000 b/s	1,544,000 b/s
+ DS1 bit stuffing rate	1,796 b/s	393 b/s
= "intermediate" DS1 rate	1,545,796 b/s	1,544,393 b/s
x 4 DS1s per DS2	4	4
= subtotal	6,183,184 b/s	6,177,572 b/s
+ DS2 OH rate	128,816 b/s	128,699 b/s
= nominal DS2 rate	6,312,000 b/s	6,306,272 b/s
+ DS2 bit stuffing rate	3,671 b/s	9,398 b/s
= "intermediate" DS2 rate	6,315,671 b/s	6,315,671 b/s
x 7 DS2s per DS3	7	7
= subtotal	44,209,694 b/s	44,209,694 b/s
+ DS3 OH rate	526,306 b/s	526,306 b/s
= nominal DS3 rate	44,736,000 b/s	44,736,000 b/s

Figure 11
M13 format vs. C-bit format: progression from nominal DS1 to nominal DS3.

NOTE:
The calculations are not exact because each "intermediate" result is rounded off to the nearest whole number.

Appendix D: DS1, DS2, and DS3 Specification Summary

DS1

Line Rate:
1,544,000 b/s

Channels:
24 8-bit DS0 channels/frame

OH Bits:
1 per frame

Total Bits:
193 bits/frame

DS2

Line Rate (M13 format):
6,312,000 b/s

"Pseudo" Line Rate (C-bit parity format):
6,306,272 b/s

Signals:
4 DS1 signals

OH Bits:
24 bits total/frame

F-bits (framing)	8 bits/frame
M-bits (multiframing)	4 bits/frame
C-bits (stuffing)	12 bits/frame
Data bits between OH bits	48

OH Bit Sequence:
M_0 [48] C_{11} [48] F_0 [48] C_{12} [48] C_{13} [48] F_1
M_1 [48] C_{21} [48] F_0 [48] C_{22} [48] C_{23} [48] F_1
M_1 [48] C_{31} [48] F_0 [48] C_{32} [48] C_{33} [48] F_1
M_x [48] C_{31} [48] F_0 [48] C_{42} [48] C_{43} [48] F_1

Total Bits:
1,176 bits/frame

Total DS1 Information Bits:
1,152 bits/frame

Frame:
4 subframes

Subframe:
6 blocks

Block:
49 bits (48 data bits and 1 OH bit)

Frame Alignment Pattern (F-bits):
"01" every subframe

Multiframe Alignment Pattern (M-bits):
"011X" every frame

OH Bit Rate:
128,816 b/s (M13 format)

Stuffing Rates per DS1:
Maximum:
5,367 b/s (DS1 min. rate = 1,540,429 b/s)
Nominal (M13 format):
1,796 b/s (DS1 nom. rate = 1,544,000 b/s)
Nominal (C-bit format):
393 b/s (DS1 nom. rate = 1,544,000 b/s)
Minimum:
0 b/s (DS1 max. rate = 1,545,796 b/s)

DS3

Line Rate:
44,736,000 b/s

Signals:
7 DS2 signals = 28 DS1 signals

OH Bits:
56 bits total/frame

F-bits (framing)	28 bits/frame
M-bits (multiframing)	3 bits/frame
C-bits (stuffing)	21 bits/frame
X-bits (message)	2 bits/frame
P-bits (parity)	2 bits/frame
Data bits between OH bits	84

OH Bit Sequence:

X [84] F_1 [84] C_{11} [84] F_0 [84] C_{12} [84] F_0 [84] C_{13} [84] F_1
X [84] F_1 [84] C_{21} [84] F_0 [84] C_{22} [84] F_0 [84] C_{23} [84] F_1
P [84] F_1 [84] C_{31} [84] F_0 [84] C_{32} [84] F_0 [84] C_{33} [84] F_1
P [84] F_1 [84] C_{41} [84] F_0 [84] C_{42} [84] F_0 [84] C_{43} [84] F_1
M_0 [84] F_1 [84] C_{51} [84] F_0 [84] C_{52} [84] F_0 [84] C_{53} [84] F_1
M_1 [84] F_1 [84] C_{61} [84] F_0 [84] C_{62} [84] F_0 [84] C_{63} [84] F_1
M_0 [84] F_1 [84] C_{71} [84] F_0 [84] C_{72} [84] F_0 [84] C_{73} [84] F_1

Total Bits:
4,760 bits/frame

Total DS2 Information Bits:
4,704 bits/frame

Frame:
7 subframes

Subframe:
8 blocks

Block:
85 bits (84 data bits and 1 OH bit)

Frame Alignment Pattern (F-bits):
"1001" every subframe

Multiframe Alignment Pattern (M-bits):
"010" every frame

OH Bit Rate:
526,306 b/s

Stuffing Rates per DS2:
Maximum[1]:
9,398 b/s (DS2 min. rate = 6,306,272 b/s)
Nominal:
3,671 b/s (DS2 nom. rate = 6,312,000 b/s)
Minimum:
0 b/s (DS2 max. rate = 6,315,671 b/s)

[1]Stuffing is always set for the maximum rate for the C-bit parity format.

Notes

!! DO NOT PRINT THIS PAGE !!

DS2 input 1 = 6,3
Stuffing

DS2 input 2 = 6
St

DS2 input 3
Stu

DS2 input
S

DS2 inp

DS2 i

DS

D

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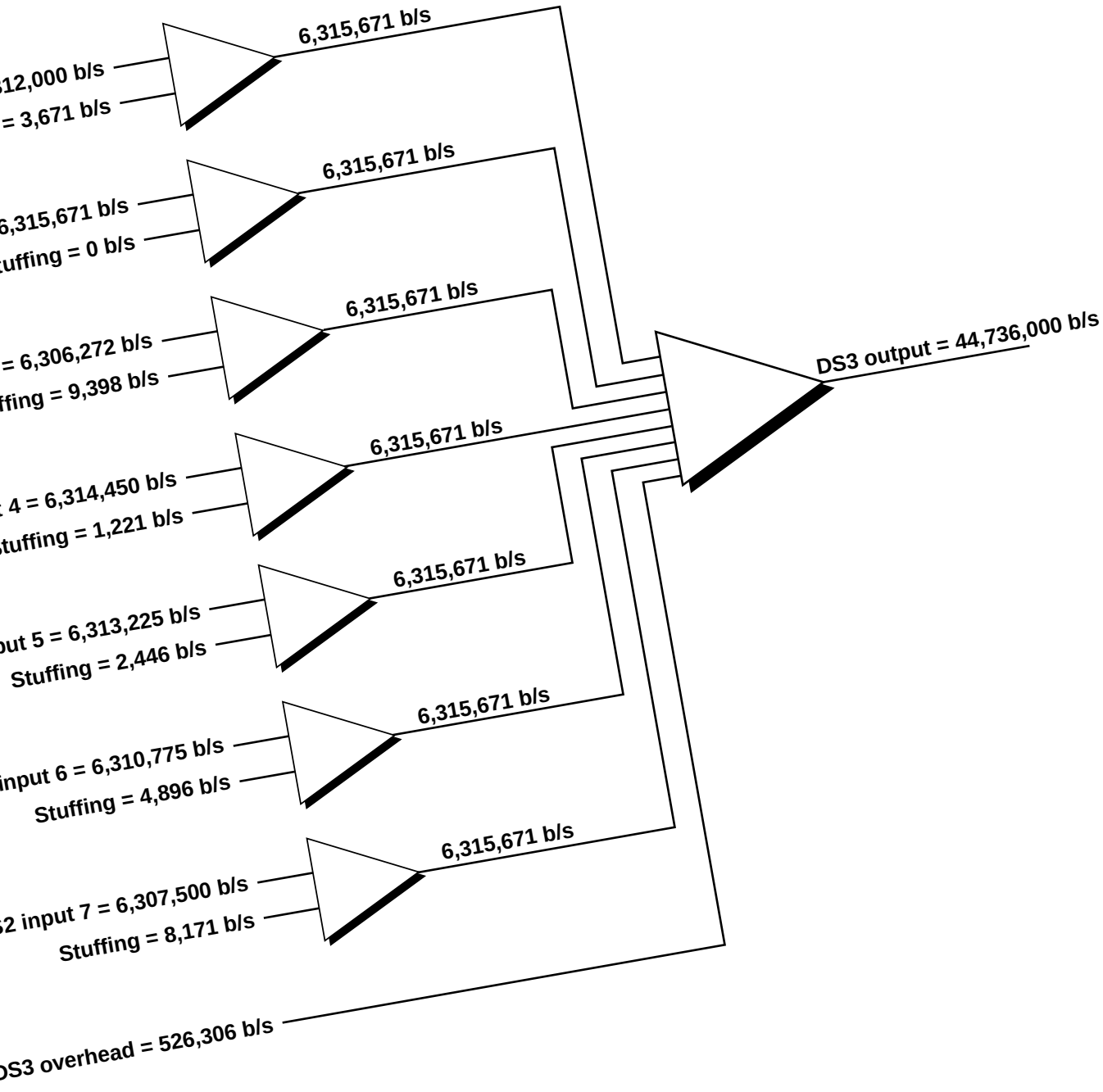
The Fundamentals of DS3

Technical Note



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