VOL. 5

E1
Pocket Guide

The World of E1

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Pocket Guide to The world of E1

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INTRODUCTION

10th March 1876: "Mr Watson, come here. I want you!"

This was the first complete sentence spoken by Alexander Graham Bell using his patented telephone. By the end of 1876 the first long distance two-way telephone conversation took place and in 1877 the first telephones were available for rental.

The telephone system was born and grew fairly rapidly. Even today voice communication still forms the major part of the total volume of the communication traffic.

The aim of communications systems has been to get more and more information transmitted on a single cable. This involves gathering a number of sources together, transmitting them together and then separating them and passing them to the individual receivers.

One of the methods used is Frequency Division Multiplexing (FDM). Here a set of telephone channels are modulated with different carrier frequencies to shift the signals into a different frequency range. In this analogue system each channel is separated by frequency.

With ever increasing demands for higher transmission rates with better quality and at lower costs other systems were developed. In the 1960s, digital systems started to appear. Here the telephone channels are separated by time using the method known as Pulse Code Modulation (PCM).

Towards the end of the 1980s, Synchronous Digital Hierarchy (SDH) was introduced. This created networks that can easily be adapted to meet the ever growing demand for 'bandwidth hungry' applications and services.

The aim of this booklet is to provide information on the 2Mbit/s (E1) PCM system which is the building block for modern digital communication systems

PCM COMMUNICATION SYSTEMS

The plesiochronous digital hierarchy (PDH) has two primary communication systems as its foundation. These are the T1 system based on 1544kbit/s that is recommended by ANSI and the E1 system based on 2048kbit/s that is recommended by ITU-T.

The T1 system is used mainly in the USA, Canada and Japan. European and certain non-European countries use the E1 system.

	Common characteristics	**E1 and T1**
a	Sampling frequency	8kHz
b	Number of samples per telephone signal	8000 per second
c	Length of PCM frame	1/b = 1/8000/s = 125μs
d	Number of bits in each code word	8
e	Telephone channel bit rate	b x d = 8000/s x 8 bit = 64kbit/s

	Differing characteristics	E1	T1
f	Encoding/decoding Number of segments in characteristic	A-law 13	µ-law 15
g	Number of timeslots per PCM frame	 32	 24
h	Number of bits per PCM frame (* signifies an additional bit)	d x g = 8 x 32 = 256 bits	d x g + 1* = 8 x 24 + 1* = 193 bits
i	Length of an 8-bit timeslot	(c x d)/h = (125µs x 8)/256 = approx. 3.9µs	(c x d)/h = (125µs x 8)/193 = approx. 5.2µs
k	Bit rate of time-division multiplexed signal	b x h 8000/s x 256 bits 2048kbit/s	b x h 8000/s x 193 bits 1544kbit/s

Table 1: Characteristics of the E1 and T1 communication systems

The special features and characteristics of the E1 system are described in the following pages.

PCM SIGNAL

The analogue signal (speech) from the telephone is first converted to a Pulse Amplitude Modulated (PAM) signal using a process called sampling.

Then using quantisation and encoding this sampled analogue (PAM) signal is converted to a digital PCM Signal.

Sampling

Sampling is the periodical measurement of the value of the analogue signal.

A sampled signal contains all the information if the sampling frequency is at least twice the highest frequency of the signal to be sampled, Shannon's sampling theorem.

As the analogue signals in telephony are band-limited from 300 to 3400Hz, a sampling frequency of 8000Hz, one sample every 125µsec, is sufficient.

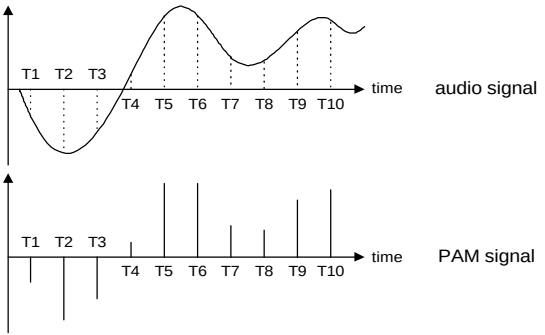


Figure 1 - Time and frequency domain of the analogue and PAM signals

Quantisation and Encoding

In the E1 system, the PAM signals are quantised using a 13-segment compression characteristic known as the A-law which is governed by the following expression:

$$y = (1 + \ln Ax)/(1 + \ln A) \qquad \text{where } A = 87.6$$

x = normalised compressor input voltage

y = normalised compressor output voltage

This characteristic is made up of 7 different size segments for the positive and negative halves, with two segments around the zero point forming a single straight line segment. Each segment is divided into linear steps with the segments about the zero point having 32 steps and the rest having 16 steps.

This results in a non-linear quantisation of the sampled signal, which has a useful effect on the signal-to-quantising noise (S/Q) ratio.

Most of information in the human voice is at the low amplitudes and the segment about the zero point covers one sixty-fourth of the amplitude range and is divided into 32 steps. Whereas the top half of the input signals dynamic range is covered by the last 16 step segment of the characteristic.

With 128 steps for the positive and negative signal amplitudes a total of 256 steps requires 8 bits (2^8). The most significant bit is the sign bit and is set to 1 for the positive amplitudes. The next 3 bits are used for the segments with the last 4 bits for the 16 steps in each segment.

It can be seen that the S/Q ratio improves linearly over the first linear segment of the compression characteristic, and then flattens off at a value of 37 to 38dB which remains practically constant over the remaining dynamic range. In practice this means that there is a constant S/Q ratio over the normal amplitude range for speech signals from around 33dBm0 to -5dBm0, resulting in good intelligibility of the speech signals transmitted in this way.

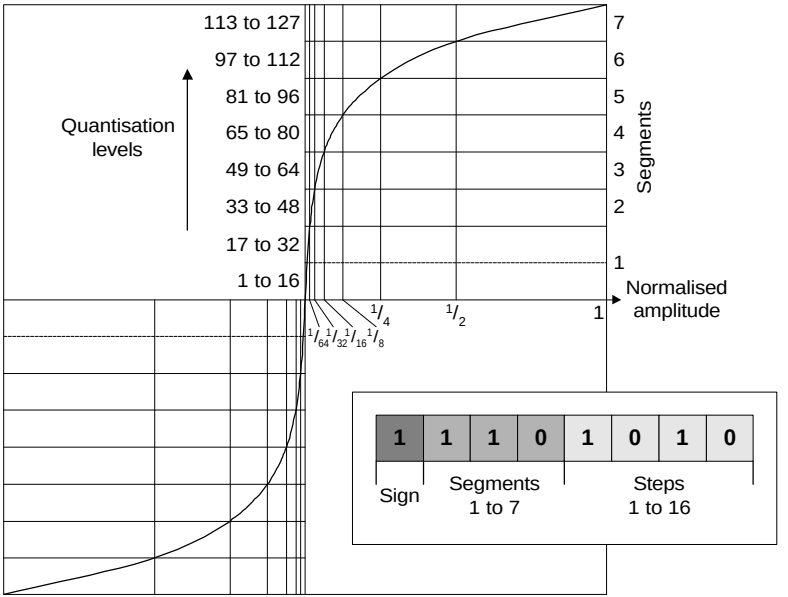


Figure 2: 13-segment compression characteristic to ITU-T Recommendation G.711

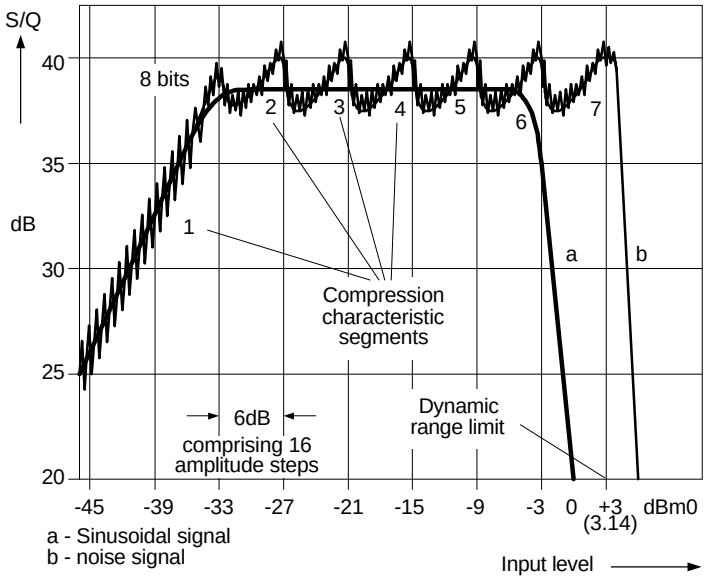


Figure 3: Characteristic signal-to-quantising-noise (S/Q) ratio curves

PCM FRAMING

Principles of multiplexing

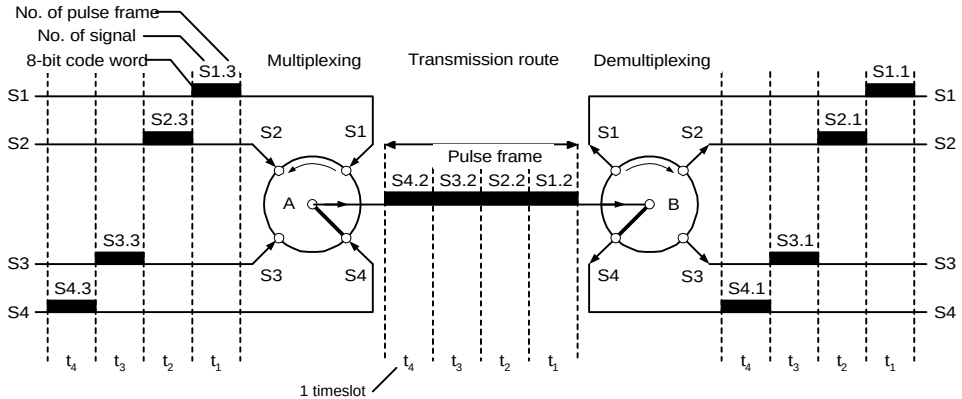


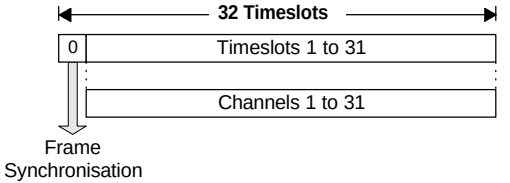
Figure 4: Principle of time-division multiplexing

Source coding produces 8-bit code words at a rate of 8kHz for each speech channel, giving 64kbit/s which can then be transmitted. To improve the utilisation of the transmission medium, the signals are transmitted by time-division multiplexing, where the code words are interleaved and contained in a pulse code modulation (PCM) frame. The figure above shows the principle of time-division

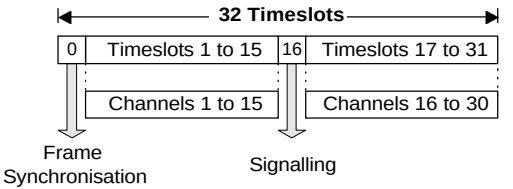
multiplexing as illustrated by the transmission of four digital signals.

The Primary Frame

A primary frame consists of 32 code words called timeslots and are numbered 0 to 31. A PCM31 frame comprises of 31 timeslots used for traffic and 1 timeslot used for synchronisation.



In a PCM30 system the frame comprises of 30 timeslots used for traffic and 2 code words that are used for synchronisation and signalling purposes.



Frame alignment

The transmitting and receiving sides are synchronised to the PCM frame with the aid of the Frame Alignment Signal (FAS) which is transmitted in timeslot 0 of every second frame. The Not Frame Alignment Signal (NFAS) is transmitted in timeslot 0 of the alternate frames.

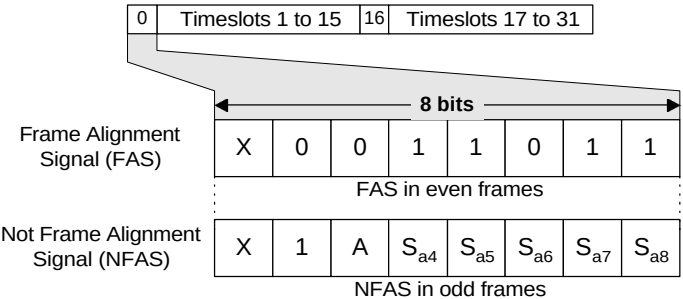


Figure 5: The FAS and NFAS Signals

Frame Alignment Signal (FAS)

Bit number	1	2	3	4	5	6	7	8
Binary value	S_i (C)	0	0	1	1	0	1	1

bit 1: S_i is reserved for international use, in PCM30 or PCM31 or

C is used for transmitting the CRC division remainder in PCM30C or PCM31C

bits 2 to 8: FAS

The receiving side of the PCM system determines the timeslots of the PCM frame on the basis of the received frame alignment signals, so that the received bits can be assigned to the various channels in the correct sequence.

The FAS is transmitted in timeslot 0 of every *even* PCM frame, i.e. frame numbers 0, 2, 4, 6, and so on. It is always a 7 bit word with the binary sequence 001101 starting at bit 2.

Bit 1 in timeslot 0 is known as the S_i bit and is reserved for international use. It is normally set the 1 except in systems that use CRC. Here the division remainder which results from the comparison is transmitted to the receiving side using this bit.

Not Frame Alignment Signal (NFAS)

The NFAS is used to carry information about the status of the link and to provide control signals for primary rate multiplexers

Bit number	1	2	3	4	5	6	7	8
Binary value	S_i (M)	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}

bit 1: S_i is reserved for international use, in PCM30 or PCM31 or

M is used for transmitting the CRC-multiframe alignment signal in PCM30C or PCM31C;

bit 2: is set to 1 - prevents simulation of the FAS;

bit 3: A shows the remote alarm indication.

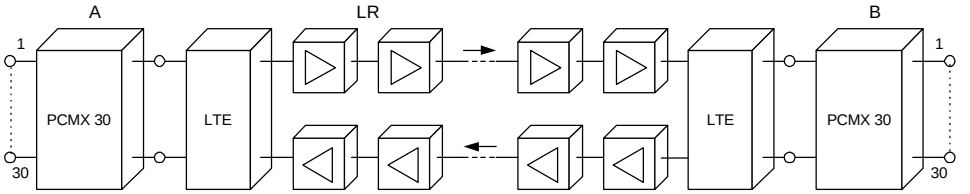
bits 4 to 8: S_{a4} to S_{a8} are additional spare bits which can be used as follows:

Sa bits

ITU-T Recommendations allow for bits S_{a4} to S_{a8} to be used in specific point-to-point applications (e.g. for transcoder equipment) within national borders. When these bits are not used and on links crossing an international border they should be set to 1.

Bit S_{a4} may be used as a message-based data link for operations, maintenance and performance monitoring. This channel originates at the point where the frame is generated and terminates where the frame is split up.

Frame Synchronisation



PCMX 30 = Primary Multiplexer for 30 speech/data channels
LTE = Line Terminating Equipment
LR = Line Regenerator

Figure 6: 2048kbit/s transmission system

Considering the multiplexers in the above diagram.

PCM multiplexer B will synchronise on to the incoming bit stream from multiplexer A under the following conditions:

1. Correct FAS, S_i 0 0 1 1 0 1 1, is received in timeslot 0 of a frame.
2. Bit 2 in timeslot 0 (NFAS) of the next frame received must be 1, S_i 1 A S_{a4} S_{a5} S_{a6} S_{a7} S_{a8}, is received in timeslot 0.
3. FAS, S_i 0 0 1 1 0 1 1, is received in timeslot 0 of the subsequent frame.

The multiplexer is synchronised on to the incoming frames only if *all three* conditions are fulfilled.

SIGNALLING

In PCM30 and PCM30C systems timeslot 16 is used for channel-associated signalling (CAS). The information necessary for switching and routing all 30 telephone channels (signalling and status codes) are interleaved and transmitted in this timeslot.

The interchange of signalling between the multiplexers in the forward and backward channel takes place using pulse signals comprising four bits (a, b, c, d) which are formed by signalling multiplex equipment from the signals originating in the exchange. One example of a signalling method is Exchange and Multiplex (E & M) signalling.

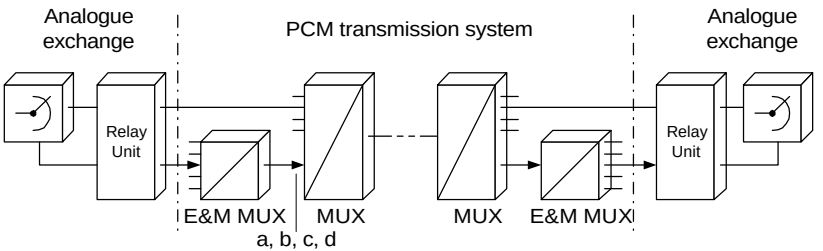


Figure 7: E & M signalling

E & M signalling

In this method, relay units are used to match the signals coming from the exchange to the E & M equipment. The E & M multiplexer detects the signalling, converts it into 4-bit signals and passes these on to the PCM multiplexer for insertion into timeslot 16 of the PCM frame.

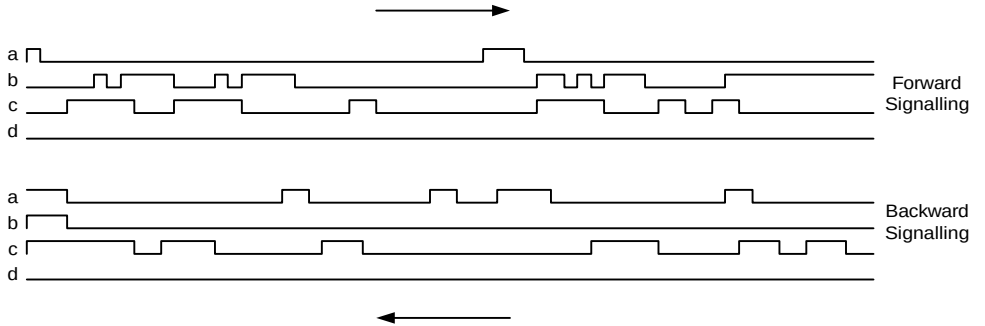


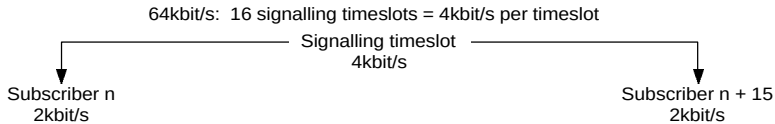
Figure 8: Channel-associated signalling (CAS)

Channel-associated signalling (CAS)

Interchange of signalling in the forward and backward directions is accomplished using bits that only change state slowly. It is therefore sufficient to transmit these relatively static signalling bits at a rate of 2kbit/s for each subscriber.

As a result, the 64kbit/s capacity of timeslot 16 is divided between the 30 subscriber channels and 2 auxiliary channels for synchronisation and alarms. A signalling multiframe is formed which comprises 16 normal PCM frames.

Each signalling timeslot of the multiframe has a transmission capacity of 4kbit/s (64kbit/s divided into 16 frames). Each of these timeslots is sub-divided to include 2 subscriber channels, giving a signalling rate per channel of 2kbit/s.



Signalling Multiframe

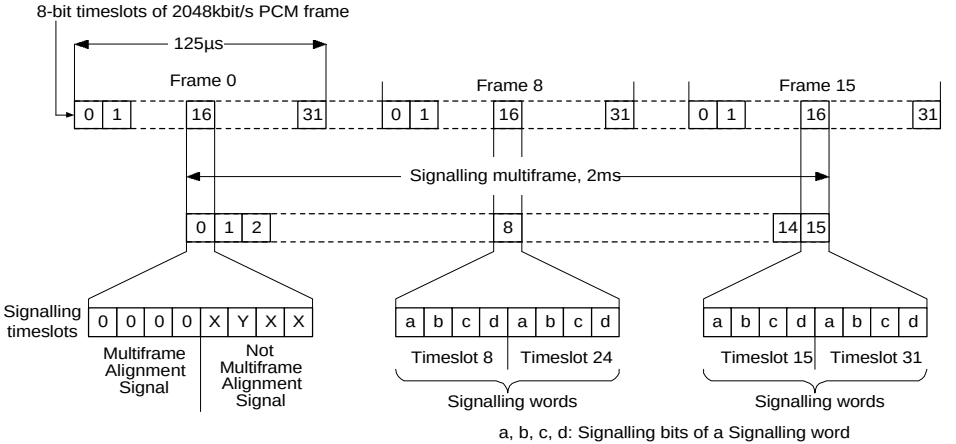


Figure 9: Signalling multiframe

The first four bits in timeslot 16 of the first frame (frame 0) of the signalling multiframe are used to transmit the Multiframe Alignment Signal (MFAS) = 0 0 0 0. The last four bits contain the Not Multiframe Alignment Signal (NMFAS) = X Y X X. The signalling multiframe structure is as shown in the table below:

frame number	Bits in channel timeslot 16	
	a b c d	a b c d
0	0 0 0 0	X Y X X
1	Telephone channel 1	Telephone channel 16
2	Telephone channel 2	Telephone channel 17
3	Telephone channel 3	Telephone channel 18
4	Telephone channel 4	Telephone channel 19
5	Telephone channel 5	Telephone channel 20
6	Telephone channel 6	Telephone channel 21
7	Telephone channel 7	Telephone channel 22
8	Telephone channel 8	Telephone channel 23
9	Telephone channel 9	Telephone channel 24
10	Telephone channel 10	Telephone channel 25
11	Telephone channel 11	Telephone channel 26
12	Telephone channel 12	Telephone channel 27
13	Telephone channel 13	Telephone channel 28
14	Telephone channel 14	Telephone channel 29
15	Telephone channel 15	Telephone channel 30

0 0 0 0 = multiframe alignment signal

X = reserved bit normally set to 1; Y = distant multiframe alarm bit

Table 2: Assignment of bits in timeslot 16 of a signalling multiframe for channel- associated signalling

Pulse Dialling

Since only timeslot 16 is used for CAS and 16 PCM frames are linked together to form a signalling multiframe, it follows that this multiframe has a length of 16 x 125µs = 2ms. This means that the signalling information for all 30 subscribers are transmitted in a period of 2ms and that the signalling information for each subscriber is updated every 2ms. This is sufficient, since the shortest signalling pulses are the dialling pulses which have a pulse length to pause ratio of 40 to 60ms which is long in comparison to the 2ms sampling interval.

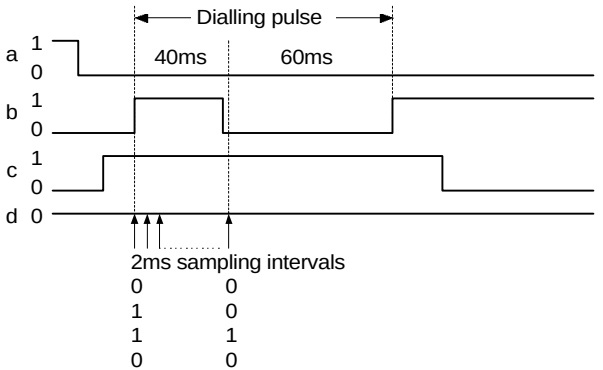


Figure 10: Updating the signalling information at 2ms sampling intervals

CYCLIC REDUNDANCY CHECK (CRC)

With the introduction of ISDN (Integrated Services Digital Network), subscribers are provided with transparent 64kbit/s channels for speech or data transmission. Transparent in this sense means that the binary signal transmitted by the subscriber is transmitted over the entire signal path without being altered in any way by analogue/digital conversion or other means, with the bit sequence integrity preserved.

There is a danger with this type of data communication that the subscriber may intentionally or unintentionally transmit the bit pattern 10011011 which corresponds to the FAS. This may lead to the PCM multiplexer re-synchronising to this apparent FAS, with the result that all of the PCM channels will be incorrectly assigned.

To avoid this disastrous malfunction of the system, ITU-T Recommendation G.704 specifies the use of the CRC-4 cyclic redundancy check for 2048kbit/s systems. These are also known as PCM30C and PCM31C systems.

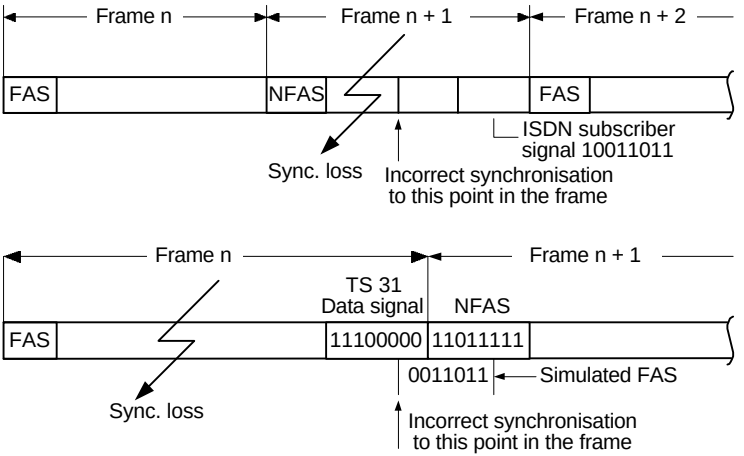
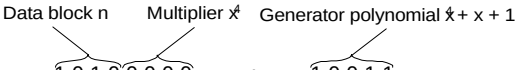


Figure 11: Examples of incorrect synchronisation caused by simulation of the frame alignment signal

CRC-4 method

The transmitting side of the PCM multiplexer forms a CRC check block (block n) from eight consecutive PCM frames. This block contains 2048 bits (8 x 256 bits). The check block is multiplied by x^4 and then divided by the generator polynomial $x^4 + x + 1$.

Example of the CRC-4 calculation:



The remainder from the division process, is also called the system signature, and comprises of 4 bits. These are written into bit 1 in the frame alignment signals of the next data block (n + 1) as the bits designated C_1, C_2, C_3 and C_4.

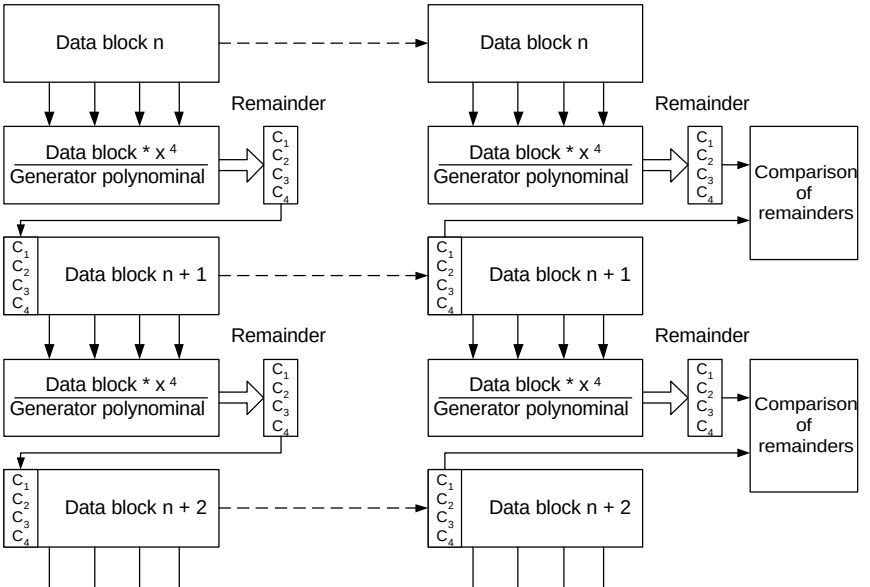
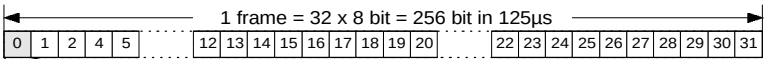


Figure 12: Schematic diagram of CRC-4 function

After this, data block n is transmitted to the receiving side and again subjected to the same multiplication and division process from which get a 4 bit remainder.

When data block n+1 is transmitted, the remainder from dividing data block n on the transmitting side is also transmitted to the receiving side, where it is compared with the remainder from dividing data block n on the receiving side. If the two remainders are identical, no bit errors have occurred during transmission. If there is a difference between the two remainders, it can only mean that the received block has been degraded by one or more bit errors during transmission.

CRC multiframe



Sub-multi-frame No.	Frame No.		1	2	3	4	5	6	7	8
I	0	FAS	C_1	0	0	1	1	0	1	1
	1	NFAS	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	2	FAS	C_2	0	0	1	1	0	1	1
	3	NFAS	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	4	FAS	C_3	0	0	1	1	0	1	1
	5	NFAS	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	6	FAS	C_4	0	0	1	1	0	1	1
	7	NFAS	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
II	8	FAS	C_1	0	0	1	1	0	1	1
	9	NFAS	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	10	FAS	C_2	0	0	1	1	0	1	1
	11	NFAS	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	12	FAS	C_3	0	0	1	1	0	1	1
	13	NFAS	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	14	FAS	C_4	0	0	1	1	0	1	1
	15	NFAS	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}

CRC multiframe

FAS = Frame Alignment Signal 0011011

NFAS = Not Frame Alignment Signal

C_1 to C_4 = Cyclic Redundancy Check 4 bits

E = CRC-4 error indication bits

A = Remote alarm indication

S_{a4} to S_{a8} = Spare bits

Figure 13: CRC-4 multiframes

Transmission of the remainder requires a capacity that is obtained by making use of the otherwise redundant bit 1 in the FAS of each even-numbered frame. To locate the four check bits C_1, C_2, C_3, C_4 making the remainder, a CRC multiframe is formed.

The CRC-4 multiframe consists of 16 PCM frames just like the signalling multiframe and therefore also has a duration of 2ms. This multiframe is divided into two 8 framed sub-multiframes, I and II. A CRC Multiframe Alignment Signal (CRC MFAS) is used to synchronise the receiving side to this multiframe.

The CRC MFAS is a 6-bit signal of 0 0 1 0 1 1 and is inserted bit-by-bit into the first bit of the NFAS in frames 1, 3, 5, 7, 9 and 11. The first bits of frames 13 and 15 are called the E bits and are used to indicate the data blocks with bit errors back to the transmitting side. If the E bit in frame 13 = 0 it indicates that there is a CRC error in the data contained in sub-multiframe I and if the E bit in frame 15 is 0 it indicates the same situation for sub-multiframe II. These E bit errors are also called remote or distant CRC errors.

As each CRC sub-multiframe comprises 8 standard PCM frames it is therefore 8 x 125µs = 1ms long so the system carries out 1000 CRC comparisons per second. When compared with the monitoring of the FAS as carried out in systems without CRC, the CRC system has the advantage of a greater degree of certainty in the detection of possible errors because all of the transmitted data is monitored.

The system without CRC monitors only a small part of the signal, namely 7 bits for every 505 bits. The CRC method does not, however, detect all possible errors. A multiple error in a CRC block may lead to the formation of the correct signature, even though the block contains errors. Since the CRC remainder is a 4-bit word, it follows that 1/16th or 6.25% of the blocks may contain errors, despite a correct signature. In other words, the certainty with which an error can be detected is 93.75% of the total number of errors.

The standard procedure used in data communications of repeating any data blocks containing errors is not possible in PCM transmissions, since the data is not buffered at any point.

The CRC method cannot accurately determine single errors as it is not possible to say how many errors were the cause of an incorrect remainder in the check sum. The result is therefore a “greater than” result, which is sufficient, since the continuous monitoring makes it possible to keep a constant watch on the transmission quality.

Frame synchronisation (with CRC-4)

A transmission system utilising CRC-4 carries out 1000 CRC comparisons every second. If the number of negative (incorrect) comparisons exceeds a threshold of 914 in 1000 (91.4%), the system goes out of synchronisation. Resynchronisation takes place in the following manner:

1. Normal synchronisation of the PCM system
   a) Frame alignment signal correctly received
   b) Second bit in the NFAS must be 1
   c) Next FAS also received correctly.
2. Synchronisation of the CRC multiframe
   Bit position 1 of the NFAS contained in the frames of the CRC multiframe is checked for the CRC multiframe alignment signal of 0 0 1 0 1 1

CRC multiframe synchronisation is achieved when at least 2 CRC MFAS have been correctly received within a period of 8ms, (4 CRC submultiframes). Between these two correct CRC MFAS there must be 2ms or a multiples thereof.

Only when the conditions 1 and 2 above are fulfilled is the system synchronised and CRC calculations commence.

ALARMS

Remote Alarms

Multiplexers are connected together so the PCM transmissions take place in both directions, it also follows that alarm messages are also transmitted bi-directionally.

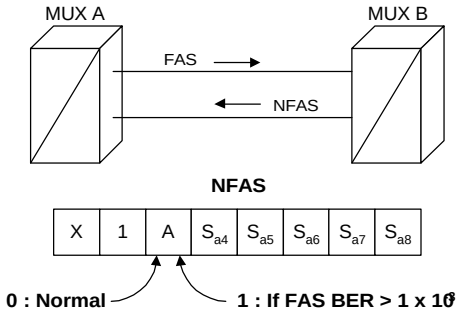


Figure 14: Alarm messages

Remote Alarm Indication

The NFAS is used to transmit service information. Bit 3 of the NFAS indicates a remote (or distant) alarm:

If Bit 3 is 0 - means undisturbed operation; no alarm.

If 1 - means that one of the following alarm situations has occurred:

Power supply failure

Codec failure

Failure of incoming 2048kbit/s signal

Frame alignment error

Frame alignment signal bit error ratio >1 x 10^{-3}.

The multiplexer located at point B continuously monitors the incoming FAS for bit errors. The FAS is received in timeslot 0 of alternate frames which is every 250µs or 4000 times per second. If the result of the bit error measurement of the FAS is ≤1 x 10^{-3}, transmission is undisturbed. The NFAS transmitted back to point A will be S_i 1 0 1 1 1 1 1.

When the FAS bit error ratio reaches a value of greater than 1 x 10^{-3}, correct operation of the transmission link is no longer possible and the receiving multiplexer goes out of synchronisation. This is indicated by setting the A bit of the NFAS to 1 which results in an alarm, called a Remote Alarm Indication(RAI) or distant alarm. In this case the NFAS transmitted back to point A is S_i 1 1 1 1 1 1 1.

Alarm Indication Signal (AIS)

The multiplexer at point A registers this alarm and then stops transmitting normal speech or data signals and transmits a continuous sequence of 1s. This causes the multiplexer on point B to show an

AIS alarm. This all 1s signal maintains the clock recovery mechanism in the regenerators so that resynchronisation can be attempted as soon as the FAS bit error ratio recovers to equal to or less than 1×10^{-3}.

ITU-T defines AIS as more than 509 1s in a 512 bit block which is a signal containing less than 3 zeros in a 2 frame period. A signal with all bits in state 1 except for the FAS (001101 = 3 zeros) is not a valid AIS and should be declared as frame sync loss.

Frame sync loss

Frame sync Loss is declared in PCM30(PCM31) framing if three consecutive incorrect FAS words are received or in PCM30C(PCM31C) framing if there more than 914 CRC errors in one second.

Multiframe sync loss

If the signalling MFAS is lost then multiframe sync loss alarm is declared.

Distant multiframe alarm

If multiframe sync loss alarm is declared in one direction the Y bit in the NMFAS (bit 2) in the opposite direction is set to 1 which results in a distant multiframe alarm.

LINE CODES

There are two main functions of line coding:

- to ensure that there is sufficient timing information from the received signal
- to prevent ‘droop’

The repeater or demultiplexer derives the sampling clock from the incoming signal and the quality of this derived clock depends on the number of transitions of the incoming signal.

Droop is an effect that can occur when conveying data over a circuit which has zero dc response. The nominal constant voltage levels can drift up or down due to the capacitance of the transmission line charging and discharging. Droop results in the 'wandering' of the signal levels and is known as baseline wander.

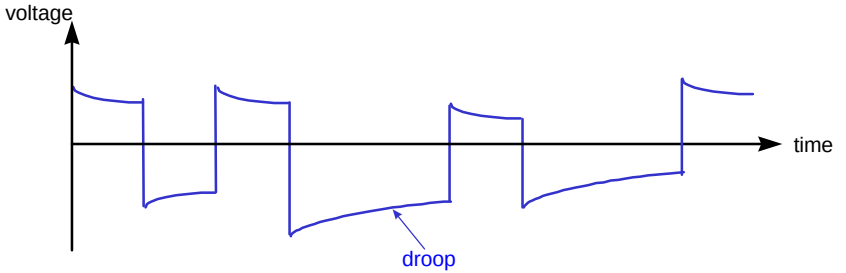


Figure 15: 'droop' on a waveform

Any zero-mean bipolar waveforms that have long strings of 1s or 0s may result in droop in the transmitted voltage level as shown above.

AMI code

Alternate Mark Inversion(AMI) is a line coding that can prevent baseline wander. Here the polarity of the signal is changed for every binary 1 of the transmitted message.

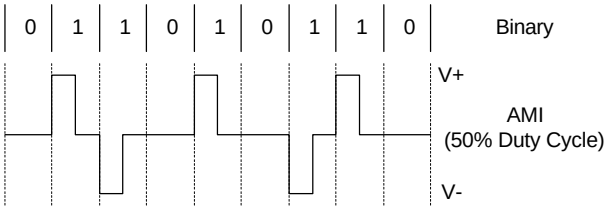


Figure 16: Showing principle of AMI

As long as the binary signal has a sufficient number of 1s then the clock signal derived from it will be suitable for the receiver to lock on to the data rate. If there are long strings of 0s then the receiver can lose synchronisation to the incoming signal.

HDB3 code

HDB3 stands for high density bipolar code in which a maximum of 3 zeros may occur in sequence. The following rules are used to convert a binary signal into a HDB3 coded signal:

Rule 1: If four 0-bits occur consecutively, the fourth zero is replaced by a violation bit or V-bit. The V-bit has the same polarity as the preceding 1-bit, which results in a violation of the AMI rule.

The substitution is thus: 0 0 0 0 becomes 0 0 0 V.

Rule 2: If there is an even number of 1-bits between the violation bit to be inserted and the previous violation bit, the first zero of the sequence of four zeros is replaced by the so-called B-bit.

The substitution is thus: 0 0 0 0 becomes B 0 0 V.

This leads to an uneven number of 1-bits, which is necessary to ensure that the inserted violation bit has the opposite polarity to the previous violation bit, so that the code remains free of any DC component.

The violation bits and B-bits must always be inserted with alternating polarity (AMI) to preserve the DC-free nature of the code.

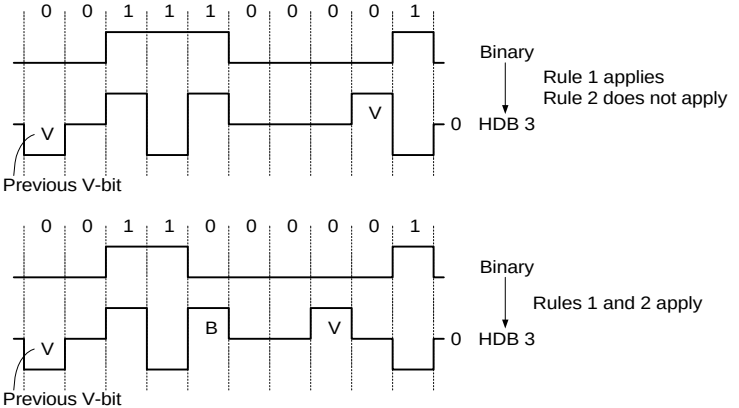


Figure 17: Examples for converting binary signals to HDB3 code

Advantages of the HDB3 code:

- The clock recovery information required for regenerators in the signal path is retained in the data signal despite long sequences of zeros
- The HDB3 code is DC-free and can therefore be transmitted using balanced, transformer-coupled circuits.

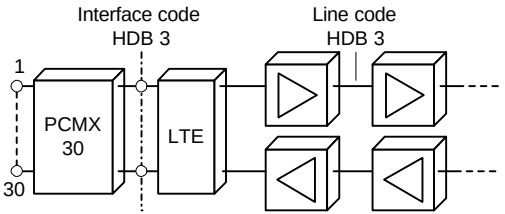


Figure 18: Interface and line codes used for 2048kbit/s transmission

ITU-T G.703 RECOMMENDATION

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see figure 15/G.703) irrespective of the sign. The value V corresponds to the nominal peak value.	
Pair(s) in each direction	One coaxial pair	One symmetrical pair
Test load impedance	75 ohms resistive	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37V	3V
Peak voltage of a space (no pulse)	0 ± 0.237V	0 ± 0.3V
Nominal pulse width	244ns	
Ratio of the amplitudes of positive and negative at the centre of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulse the nominal half amplitude	0.95 to 1.05	
Maximum peak-to-peak jitter at an output port	Refer to Section 2 of Recommendation G.823	

Table 4: Interface requirements

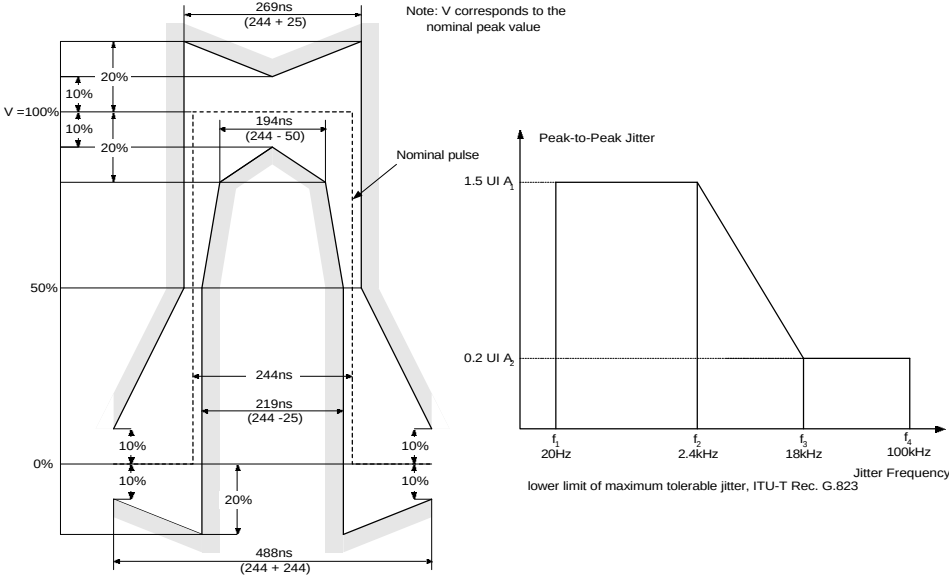


Figure 19: Mask of the pulse at the 2048kbitls interface

JITTER

Jitter is high frequency phase variations which occur, for example, when multiplexing PDH signals into SDH networks and subsequently demultiplexing them.

Types of jitter

Output jitter/intrinsic jitter:	The amplitude of the jitter present at the output of each network element.
Jitter tolerance:	Network elements must be able to tolerate a specified jitter amplitude at the input without any errors occurring, see right-hand section of Figure 14.
Jitter transfer function:	This factor indicates the degree to which jitter is amplified or attenuated by a network element.

For further information see WG booklet '*Jitter and Wander*', ref. E6.97/WGI/188/5.

APPENDIX
DATA INTERFACES

Digital signals are transmitted at a rate of 64kbit/s in data networks. These signals can be collected together to form a 2048kbit/s signal or inserted individually into such a signal. Multiplex equipment is used for this purpose. Up to thirty 64kbit/s data channels can be interleaved into the 2048kbit/s signal by the transmitting multiplexer, these being separated out on the receiving side by a corresponding demultiplexer.

The interface used between the data terminal equipment (DTE) and the data communication equipment (DCE) depends on the method used to synchronise the 64kbit/s signals to the 2048kbit/s signal. If the DTE and the multiplexer are synchronised from an external clock source, a so-called co-directional interface is used. Synchronous operation is achieved by transmitting the data signal and associated timing signal from the terminal equipment to the multiplexer.

Co-directional Interface

The term co-directional is used to describe an interface across which the information and its associated timing signal are transmitted in the same direction.

General:

Nominal bit rate: 64kbit/s

Maximum tolerance of signals transmitted across the interface: ±l00 ppm.

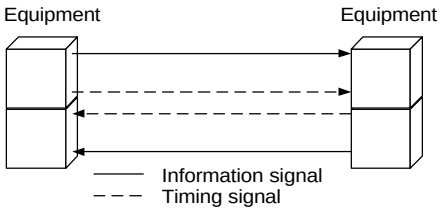
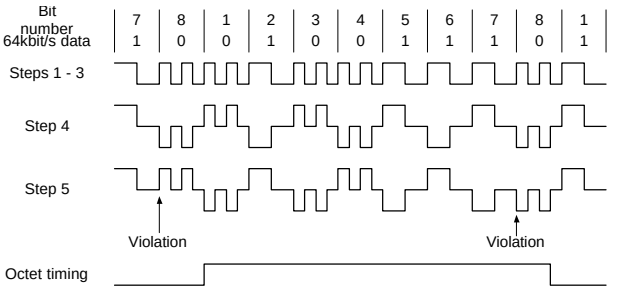


Figure 20: Co-directional interface

Code conversion rules



Step 1 - A 64kbit/s bit period is divided into four unit intervals.

Step 2 - A binary one is coded as a block of the following four bits: 1 1 0 0.

Step 3 - A binary zero is coded as a block of the following four bits: 1 0 1 0.

Step 4 - The binary signal is converted into a three-level signal by altering the polarity of consecutive blocks.

Step 5 - The alteration in polarity of the blocks is violated every 8th block. The violation block marks the last bit in an octet.

Figure 21: Code conversion rules

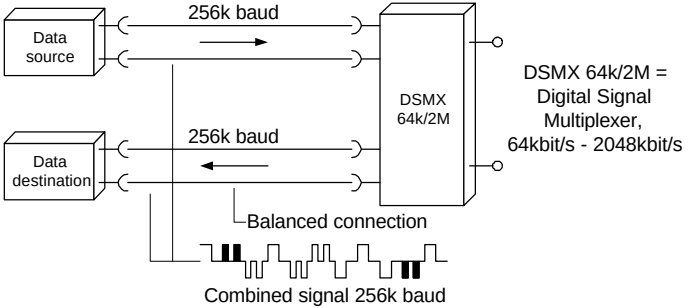


Figure 22: Example of a co-directional interface

64kHz and 8kHz timing signals are transmitted co-directionally with the information signal.

One balanced pair is used in each direction; the use of transformers is recommended.

The combined signal has a transmission speed of 256kbaud and contains the following interleaved signals

- 64kbit/s data signal
- 64kHz clock signal (signal element timing)
- 8kHz clock signal (byte timing)

Contradirectional Interface

The term contradirectional is used to describe an interface across which the timing signals associated with both directions of transmission are directed towards the subordinate equipment.

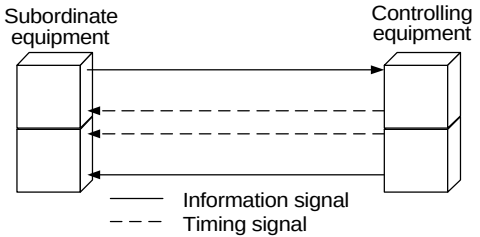


Figure 23: Contradirectional interface

General:

Bit rate: 64kbit/s.

Maximum tolerance of signals transmitted across the interface: ±100 ppm.

There should be two balanced pairs of wires for each direction of transmission, one pair carrying the data signal and the other carrying a composite timing signal (64kHz and 8kHz).

The use of transformers is recommended.

Code conversion rules

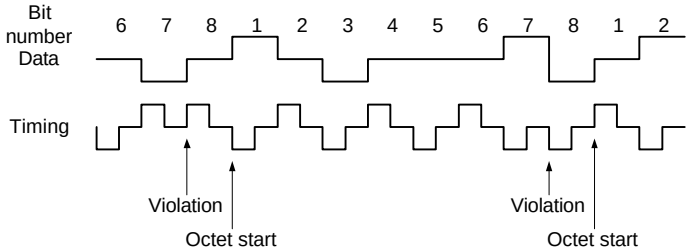


Figure 24: Code conversion rules

The data signals are AMI-coded with a 100% duty cycle. The composite timing signals convey the 64kHz signal element (bit) timing information using AMI code with a duty cycle of 50%. The 8kHz byte timing is conveyed by introducing violations of the code rule.

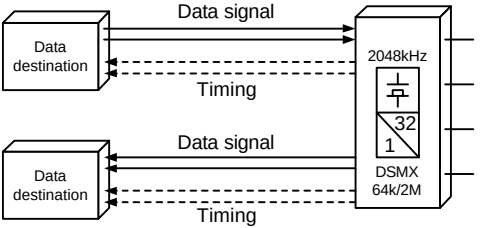


Figure 25: Example of a contradirectional interface

Use of the contradirectional interface.

End-to-end connections for 64kbit/s data signals can be produced without using external synchronisation when contradirectional interfaces are used. The multiplexer operates from its own 2048kHz clock. The 64kHz clock which is derived from this signal is used by the multiplexer to fetch the data from the terminal equipment.

PLESIOCHRONOUS DIGITAL HIERARCHY (PDH)

The greater the number of telephone channels which are collected together into a composite signal, the greater the efficiency of the telecommunications system. The signals to be transmitted are multiplexed in stages and can be switched and re-directed at any stage in the multiplexing chain, i.e. at any level in the multiplex hierarchy. This practice has resulted in a hierarchical structure based on the PCM 30 system.

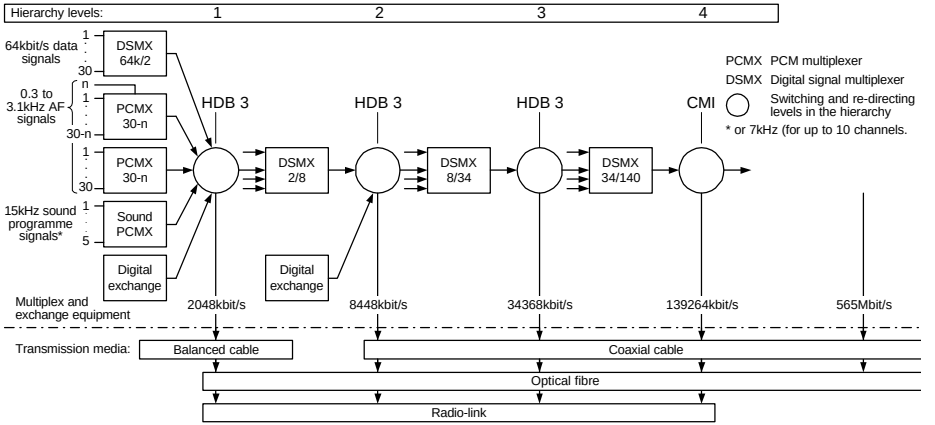


Figure 26: Hierarchy structure and transmission media used for digital communication systems

SYNCHRONOUS DIGITAL HIERARCHY (SDH)

The 1980s saw the start in the development of the synchronous digital hierarchy (SDH), with the intention of eliminating the disadvantages inherent in PDH. SDH brings the following advantages to network providers:

High transmission rates: Transmission rates of up to 10Gbit/s can be achieved in modern SDH systems. SDH is therefore the most suitable technology for backbones, which can be considered as being the super highways in today's telecommunications networks.

Simplified drop and insert function: Compared with the PDH system, it is much easier to extract and insert low-bit rate channels from or into the high speed bit in SDH.

High availability and capacity matching: With SDH, network providers can react quickly and easily to the requirements of their customers. For example, leased lines can be switched in a matter of minutes.

Reliability: Modern SDH networks include various automatic back-up and repair mechanisms to cope with system faults.

Future-proof platform for new services: SDH is the ideal platform for services ranging from POTS, ISDN and mobile radio through to data communications (LAN, WAN, etc.), and it is able to handle the very latest services such as video on demand and digital video broadcasting via ATM, that are gradually becoming established.

Interconnection: SDH makes it much easier to set up gateways between different network providers and to SONET systems. The SDH interfaces are globally standardised, making it possible to combine network elements from different manufacturers into a network.

For further information see WG SDH Pocket Guide, ref. E5.98/WGI/1006

GLOSSARY

A bit ..... remote (or distant) alarm indication
AIS ..... Alarm Indication Signal
AMI ..... Alternate Mark Inversion
ATM ..... Asynchronous Transfer Mode
CAS ..... Channel Associated Signalling
CRC-4 ..... Cyclic Redundancy Check for 2048kbit/s systems
E1 ..... 2048kbit/s PCM communication system mainly used in Europe
E&M ..... Exchange and Multiplex signalling
FAS ..... Frame Alignment Signal
G.703 ..... ITU-T Rec. For Physical/Electrical Characteristics
..... for Hierarchical Digital Interfaces
HDB3 ..... High Density Bipolar code with a maximum of 3 zeros
ISDN ..... Integrated Services Digital Network
ITU-T ..... International Telecommunication Union -
..... Telecommunication Standardisation Section
MFAS ..... Multiframe Alignment Signal
NFAS ..... Not Frame Alignment Signal

NMFAS ..... Not Multiframe Alignment Signal

PAM ..... Pulse Amplitude Modulation

PCM ..... Pulse Code Modulation

PCM30 ..... 30 channels with CAS signalling in timeslot 16

PCM30C ..... 30 channels with CAS signalling in timeslot 16 and CRC error checking

PCM31 ..... 31 channels

PCM31C ..... 31 channels with CRC error checking

PDH ..... Plesiosynchronous Digital Hierarchy

SDH ..... Synchronous Digital Hierarchy

S/Q ..... signal-to-quantising noise

SONET ..... Synchronous Optical Network

T1 ..... 1544kbit/s PCM communication system mainly used USA, Canada and Japan

Y bit ..... distant multiframe alarm bit

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