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[54] **COMMON BUS COMMUNICATION SYSTEM IN WHICH THE WIDTH OF THE ADDRESS FIELD IS GREATER THAN THE NUMBER OF LINES ON THE BUS**

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[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

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[57] **ABSTRACT**

The technique for transmitting address information between a processor and a plurality of memory subsystems in a common bus communication system. The width of the address field is greater than the number of lines on the bus. For example, addresses are three bytes wide, and the bus is one byte wide, thereby reducing the number of pins required on the processor and the subsystems. For communication between the processor and a given memory subsystem, only those bytes of a selected address which differ from the corresponding bytes of a previous address are transmitted sequentially for accessing a selected memory location.

7 Claims, 11 Drawing Figures