Design and Simulation of Addressable Failure Site Test Structure for IC Process Control Monitor

Kelvin Yih-Yuh Doong[1,2], Jye-Yen Cheng[1], Charles Ching-Hsiang Hsu[2]

[1]Worldwide Semiconductor Manufacturing Corp., Shinchu, Taiwan
[2]Microelectronics Laboratory, Semiconductor Technology & Application Research (STAR) Group,
Department of Electrical Engineering, National Tsing-Hua University, R.O.C.
TEL: 886-3-5715131 ext.4036, FAX: 886-3-5718300, Email: chhsu@ee.nthu.edu.tw

Abstract

A novel test structure to ensure failure addressable and high-density test structure of semiconductor process control monitor with a limited number of contact pads required for electrical test is described. The quiz placement and routine scheme requires only two levels of conductive layers, and provides the maximum number of bridging and continuity test structure units. A graph model is developed to manifest the spatial configuration of test structure units and simplify the complexity of fault detection. Also, a generic algorithm of multi-faults detection was developed.

Introduction

As the advance of technology development, the difficulties of semiconductor process integration increases exponentially. The application of test structures plays a key role to simply the complexity of process development, control monitor, and tracking down defect source. Yield losses from parametric causes and random defects could be easily identified by carefully characterizing the electrical test (*E-test*) of microelectronics test structures (*MTS*) [1]. However, investigation of test structure vehicles will indicate that most of layout is taken up by probe contact pads, which limits the number and effective area of test structures accommodated in the chip. Therefore, it is necessary to design a structure with minimum probe contact pads for providing relatively large area of test structures.

An approach used an addressable array for measuring line-width and step resistance [2]. A self-multiplexing scheme was proposed for the force-sense test structures [3], and a digital multiplexer was used to reduce probe contact pads [4]. The problem of these multiplexing schemes is that active devices are required. It dose not meet the requirement of short loop process. A checkerboard test structure was proposed to locate defects [5]. The arrangement of test structures is 2-D permutation and provides the maximum number of *MTS*s. However, it can not be exactly located the multi-faults of test chip [6].

To optimize the effective area of test structures and the number of probe contact pads, together with providing precise defects detection, we present a failure site addressable test structure for process development and control monitor.

Modeling of Test Structure

For the convenience of description and presentation, in this work, graphic terminology would be adopted to model the geometry of layout objects inside a test structure. The nodes ($N=\{n_1, n_2, n_3 ¡ ., n_N\}$) stand for the measuring points with conductive layout objects (conductive unit [*CU*]) like comb or meandering lines. The line (*L*) describe the measurement between two measuring pads, either short circuit check or open circuit check. $L = \{ l_{ij}, i, j=1, 2, 3 ¡ , N;$ *(a) if i1j, the* l_{ij} *means Short Circuit Check Unit (SCCU); (b) If i=j, the* l_{ij} *means Open Circuit Check Unit (OCCU);}* The whole test structure is noted by $G = (N, L)$. Hence, to identify a precise location of defect inside test chip means to access every node and identify faults inside the edges. Figure 1 shows typical test structures at the left-hand side and their geometry graphs at the right-hand side. Nodes are defined as the union of probe pads & test structures, and the non-accessible nodes are called internal nodes. For a test structure of limited nodes, the number of nodes is 8 *(N)*, the optimal solution is that the test structure contains 28 $(\frac{£P*(\ -1)}{2})$ lines for short circuit check (*SCC*) and 8 *(N)* lines for open circuit check (*OCC*) as shown in Fig. 2.

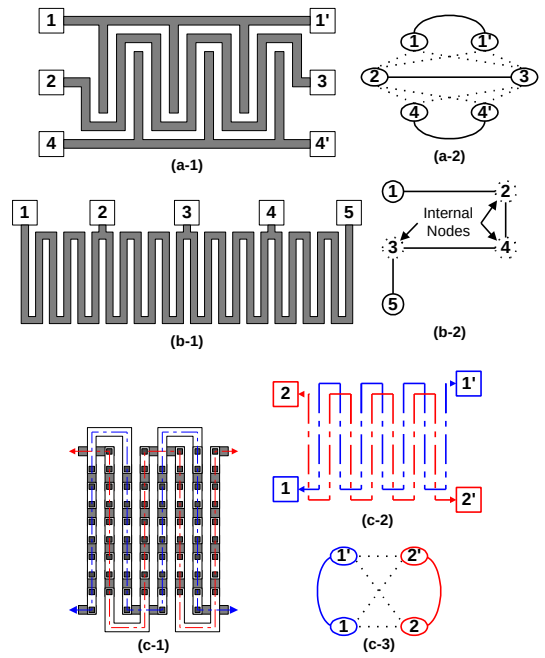

Fig. 1: Typical test structure and their geometry graphs. The solid line represents the conductive component and the dash line stands the possible leakage paths. (a-1), (b-1) Schematic layout of conductive layer. (a-2), (b-2) Geometry graph. (c-1) Schematic layout of Contact/Via chain. (c-2) Placement and routing. (c-3) Geometry graph.

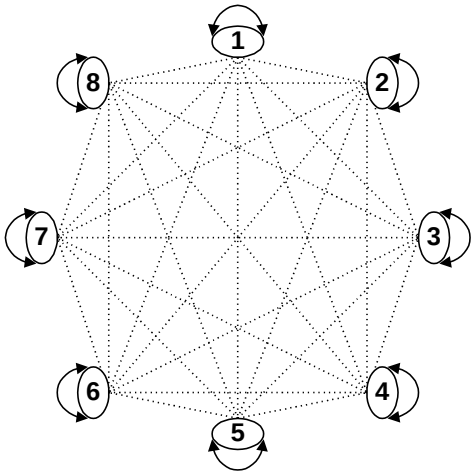

Fig. 2: Geometry graph of 8 (N)-nodes test structure.

Design of Test Structure

Routine & Placement

To implement the optimal solution of the test structure route & placement, 2-D permutation procedure is adopted to placement the units of the test structure. Figure 3 shows the location of conductive units and their neighborhood relation, respectively. Program 1 is coded to generate the 2-D permutation procedure. Figure 4 illustrates the optimal route and placement of 8-nodes test structure, and shows the unique neighborhood relation of every conductive unit *(CU)*.

$$T = \begin{matrix} \varepsilon 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 \upsilon \\ \varepsilon 2 & 4 & 1 & 6 & 3 & 8 & 5 & 7 \upsilon \\ \varepsilon 4 & 6 & 2 & 8 & 1 & 7 & 3 & 5 \upsilon \\ \varepsilon 6 & 8 & 4 & 7 & 2 & 5 & 1 & 3 \upsilon \end{matrix}$$

$$T_{n.r.} = \begin{matrix} \varepsilon(1,2) & (2,3) & (3,4) & (4,5) & (5,6) & (6,7) & (7,8) \upsilon \\ \varepsilon(2,4) & (4,1) & (1,6) & (6,3) & (3,8) & (8,5) & (5,7) \upsilon \\ \varepsilon(4,6) & (6,2) & (2,8) & (8,1) & (1,7) & (7,3) & (3,5) \upsilon \\ \varepsilon(6,8) & (8,4) & (4,7) & (7,2) & (2,5) & (5,1) & (1,3) \upsilon \end{matrix}$$

Fig. 3: The upper matrix *(T)* is the 8-nodes placement matrix and the lower matrix *($T_{n.r.}$)* shows the neighboring relation of test units inside 8-nodes test structure.

```
Clear all
K = 4;
N = 2*K;
T = zeros(K,N);
T(1,:) = 1:N;
for I = 2:K
   T(I,1) = T(I-1,2);
   T(I,N) = T(I-1,N-1);
    for J = 1:K-1
       T(I,2*J) = T(I-1,2*(J+1));
       T(I,2*J+1) = T(I-1,2*J-1);
    end;
end;
```

Program 1: The matrix *T* is generated by the above in Matlab 5.1.

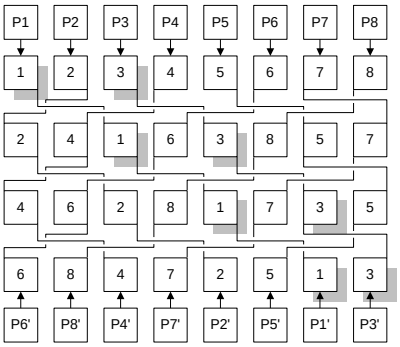

Fig. 4: Checkerboard test structure shows placement of the 8-nodes test structure.

Implementation

The test structure can be designed for monitoring dense/isolated contact/stacked via chains and conductive layers. Figure 5 presents the placement & route of this invention and its corresponding unit cell is shown in Fig. 6. The unit cell of test structure is designed to monitor the integrity of stack-via-active area module process. Standard *1P3M* logic process is employed for illustration. The layout design is based on minimum design rule *(MDR)*. To ensure the minimum yield loss from interconnection, the width & spacing of interconnection between unit cells is 3~5 times *MDR* width & spacing. The resistance between *Node-I_1*, and *Node-I_2* shows the integrity of contact & stacked-via chains. The leakage current of *Node-I*, and *Node-J* is used to detect short-circuit between *Node-I*, and *Node-J*.

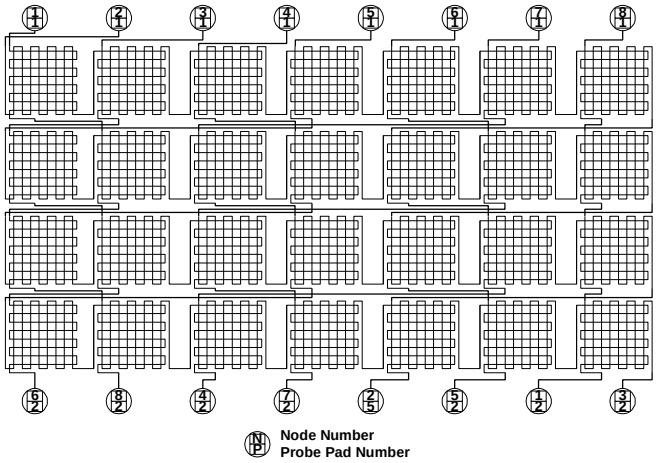

Fig. 5: Placement & route of test structure. The bold-lines present the interconnections between sub-chips (cells).

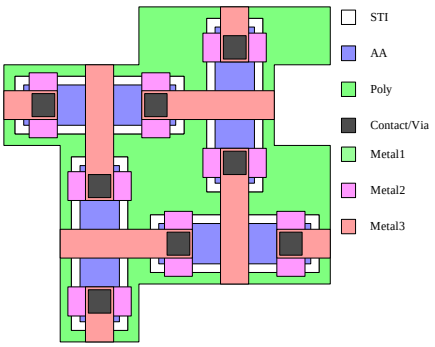

Fig. 6: Layout & schematic cross-section of unit cell.

Modeling of Fault Formation

The test structure is composed of unit-cell block modeled as resistors. The resistance of unit-cell block is the statistical measurement distribution of fault-free device. Figure 7 shows the schematic graph of short-circuit model and measurement circuit configuration. R_{inf} represents leakage from measurement system. The defect-*M* caused short-circuit between *Node-I* and *Node-J* is modeled as Rs_{m_1}, and the resistance of *Node-I* and *Node-J* are labeled as $(R_{i\_1} + R_{sm\_2})$ and $(R_{j\_1} + R_{sm\_3})$, respectively. The resistance and location of defect is generated by random number generator. The types of faults are categorized as single, tree-type, loop-type, mixed-type multi-faults shown in Fig. 8.

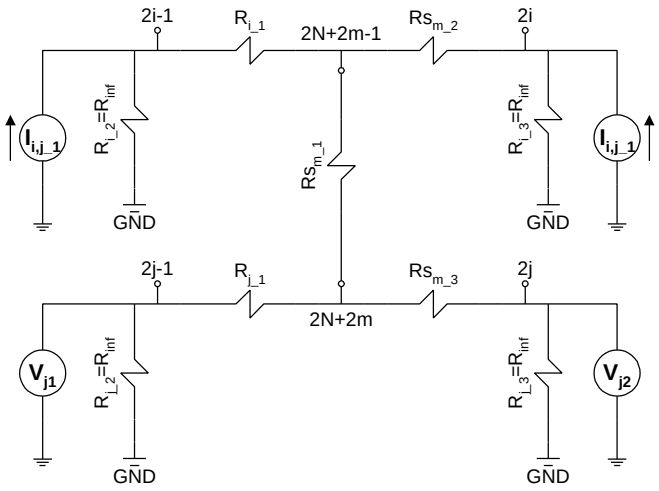

Fig. 7: Schematic graph of short-circuit model.

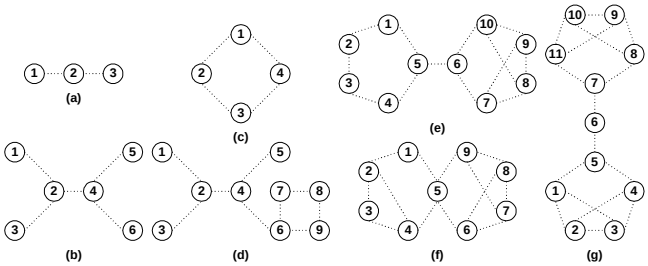

Fig. 8: Geometry graph of node configuration. (a), (b) are tree-type multi-faults. (c) is loop-type multi-faults. (d), (e), (g) is mixed- multi-faults. (f) is loop-type multi-faults.

Simulation of Fault Detection

The test structure with faults is simulated as a resistor network. The resistance of node is modeled as the statistical distribution of *E-test* measurement of fault-free device. The resistance of defect is modeled as a normal distribution, mean (m) is equal to a half of mean (m) of *E-test* measurement and standard deviation (s) is equal to the one of *E-test* measurement. A program in Matlab 5.1 was coded to solve the node voltage and the current of devices. The resistance measurement is performed at each node by forcing constant current to nodes, and voltage is measured at each of the other unforced nodes. The result is saved for off-line electrical analysis. The defect detection is composed of two parts: **defect grouping** and **single/multi fault sites identification**. The detail of testing & defect site extraction flow is shown in Fig. 9.

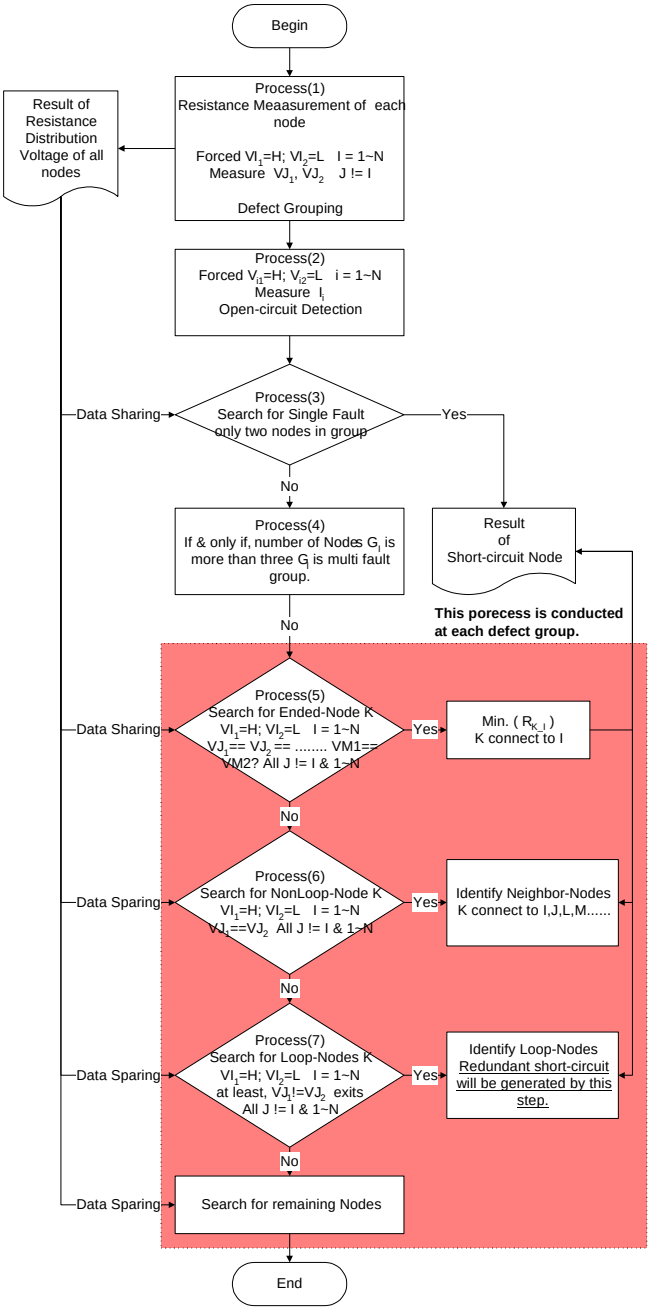

Fig. 9: Flow chart and algorithm of bridging failure detection of this novel test structure.

Results and Discussions

For validation, test structure of 80 nodes was simulated. Figure 10 presents the geometry graph of node connection. Figure 11 illustrates 3-D surface graph of leakage current between nodes, which shows all of defect sites (*Node-I & Nod-J, I, J =1~K, i 1 j*) including false defect generated measurement. Table 1 manifests the results of defect site identification. Compared with model demonstrated by Hess, et. al. [6]., this algorithm can achieve the exact defect site location. Figure 12 gives the example of this work.

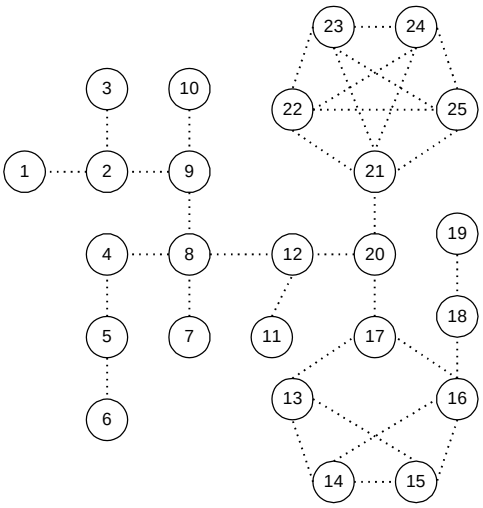

Fig. 10: Geometry graph of node configuration

Table 1: Table of node connection after defect site identification. The nodes in underline are false defect generated by algorithm of this work.

Ended Node	(1,2), (11,12), (18,19), (2,3), (5,6), (7,8), (9,10)
Non-lop Nodes	(12,20), (16,18), (17,20), (2,9), (20,21), (4,5), (4,8), (8,12), (8,9)
Loop1 Node	(21,20), (21,23), (21,24), (21,25), (22,23), (22,24), (22,25), (23,24), (23,25), (24,25)
Loop2 Node	(13,14), (13,15), (13,16), (13,17), (14,15), (14,16), (14,17), (15,16), (15,17), (16,17)

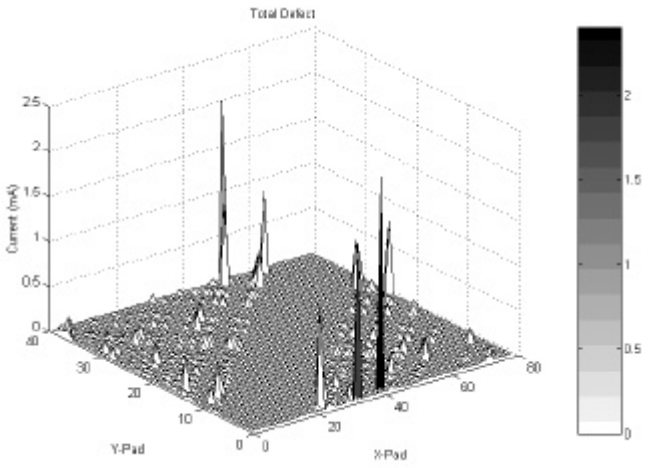

Fig. 11: 3-D surface graph of leakage current between nodes. X-axis, and Y-axis are column, and row of physical position, respectively.

Conclusion

This work provides a complete set of test structure of conductive layer and interconnection process for defect tracking method. Defects can be characterized and located prior to physical failure analysis, and the obtained defect data can be compared with the defect data obtained from inspection machine for high accurate killer ratio defining and yield prediction. By adapting this novel test structure, test chip is partitioned into sub-chip matrix. Combined the defect density from production line, area of sub-chip can be optimized to assure the low probability of more than two defects falling into same sub-chip. We proposed the methodology of systematic defect tracking & electrically automatic defect site location for timely semiconductor process development and yield monitoring of manufacturing. It also provides a promising way to correct the errors of defect data obtained by inspection machine.

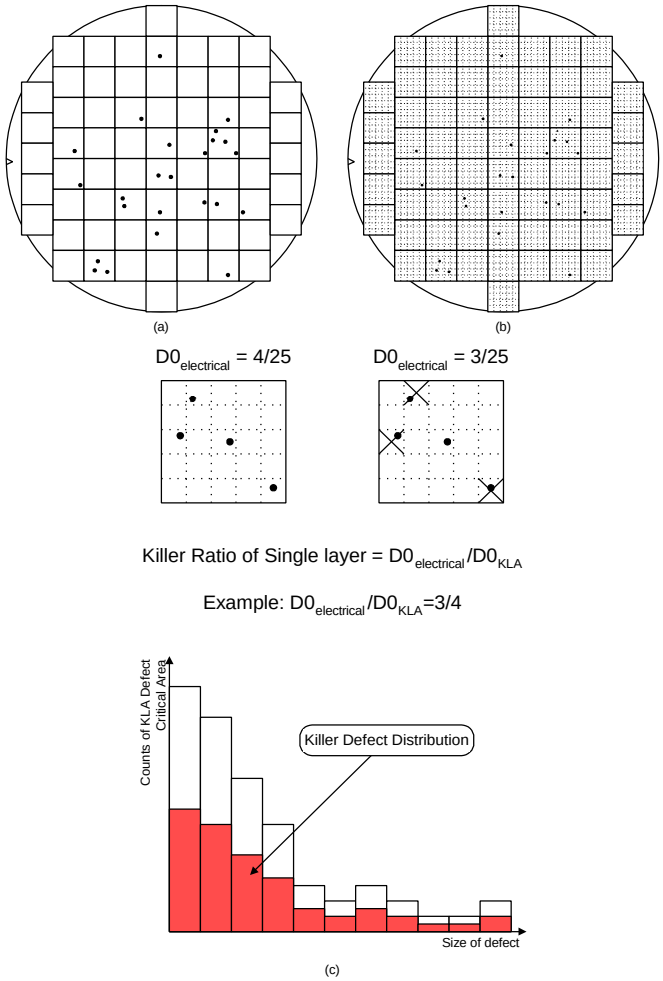

Fig. 12: (a) Defect data map from optical inspection machine. (b) *OCCUs* and *SCCUs* map from electrical parametric testing. (c) Defect distribution of yield killer as a function of defect size.

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