Mechanism and Annihilation of Shallow Trench Isolation Enhanced Poly-Mask Edge N^+/P-Well Leakage

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Abstract

The dislocation at the trench corner under Poly mask edges was found to be the major killer of junction leakage in generic logic technology. The impact of the sacrificial oxide (SAC-OX) of the well ion implantation (I/I) module and the source/drain (S/D) I/I to the defect formation are investigated for the first time. The influence of N^+/P-Well junction leakage of the I/I sacrificial oxide grown by the **R**apid **T**hermal **O**xidation (RTO) and the **F**urnace **O**xidation (FO) are evaluated on the process monitoring test structures of junction leakage. Based on the analysis of test structures and the yield evaluation of product, the optimized condition is proposed.

Introduction

Shallow trench isolation (STI) is the major isolation scheme for the quarter micron logic and memory ULSIs as well as beyond. The process-induced stress of shallow trench isolation is gotten more attention as the down-scaling of device dimension. A number of researches had pointed out the correlation between the generation of dislocation nucleation and the mechanical stress induced by the annealing thermal cycle of trench filling materials [1-4]. The N^+ S/D I/I nucleated defects is identified as the source of the trench dislocation influenced by the mechanical stress and the thermal process of S/D annealing process [5]. However, as fine tuning the 0.25 um generic logic technology, we found that the ion implantation sacrificial oxide also play a key process parameter to suppress the junction leakage of N^+/P-Well

In this work, we report the tracing of failure mechanism of N^+/P-Well junction leakage and proposed the defect-free optimized process based on the analysis of process monitor test structures of junction leakage as well as the yield evaluation of mass volume product.

Observation of Defect

The fabrication process of MOSFET with STI structures was based on the generic 0.25 £m generic logic technology. The single Poly/triple (up to five) metal logic process enacts the DUV for the active area (AA) as well as Poly gate pattern transferring and the oxide used as hard mask for AA (SiN) etching. The trenches are filled with the O_3-TEOS, followed as planarization CMP. The low temperature (750^0C) densification is enacted prior to SiN-stripped oxide dip and the high temperature (1190^0C) densification followed as the SiN-stripped, which prevent the weak seam of STI. The transistors utilized an N^+/P^+ doped Poly gate with dual gate oxide and Ti-salicide with PAI. The fully planarization 3~5 level low-k Flourinated SiO_2 (HDP)/AlCu interconnect system is used as the back end of line.

For verifying the manufacturing capability of 0.25 £m generic logic technology, hundreds lots of the test vehicle containing 512 K SRAM memory array are fabricated. At the end of line, the major yield loss is the special column failure accompanied with high standby leakage. The leakage path is identified as the junction leakage of pull-down NMOS of 6T-SRAM, moreover, the failure is only located at the Cell-A rather than Cell-B as shown in Fig. 1. Compared with the layout of Cell-A, and Cell-B, the spacing of Poly on STI to the edge of active area is 0.0 um and 0.11 um for Cell-A, and Cell-B, respectively. Figure 2 shows the SEM micrographs of Cell-A and Cell-B and the concave-shaped layout at the edge of active area NMOS/PMOS as shown in a~d. Figure 3 shows the dislocation of the failed Cell-A is located at the trench corner under the Poly mask edge.

Analysis and Process Optimization

To evaluate the impact of the I/I sacrificial oxide to the dislocation formation and the N^+/P-Well junction leakage, the SAC-OX of Well I/I is grown by furnace oxidation (T_{ox} = 9.4 nm, 750 ^{0}C) and rapid thermal oxidation (T_{ox} = 8.0/10.0/12.0 nm, 1075 ^{0}C) and the SAC-OX of S/D I/I is split into two machines (T_{ox} = 9.5/18.5 nm), which of the split conditions are shown in Fig. 4.

Figure 5 shows the characteristics of NMOSFET/PMOSFET, the narrow devices (W_G/L_G=0.35/0.25um) and the Cell-A ($W_{NG}/W_{PG}/L_G$ =2.79/1.0/0.25um). The splits do not obviously effect the sub-threshold leakage, and is free of double hump, which means the sub-threshold leakage induced by the narrow width effect is not related to the yield loss.

Four types of process monitor test structures of junction leakage are evaluated: P-1 is an area-type of AA without Poly; P-5 is a strip-type of AA without Poly; P-19 is a strip-type of AA with Poly on AA and STI, the spacing of Poly on STI to AA is 0.11 um and the width of Poly on AA/STI is 0.25 um and 0.32 um, respectively; P-20 is as same as P-19, except the width of Poly on STI is 0.36 um and the spacing of Poly to AA is 0.0 um as shown in Fig. 6. P-5, P-19 and P-20 have the same area and the peripheral length of active area. The I-V characteristics of N^+/P-Well diode are shown in Fig.7. The condition of SAC-OX of Well I/I by FO conducts higher leakage than by RTO. For P-19 and P-20, the condition of SAC-OX of Well I/I by FO conducts leakage current 3 order of magnitude higher than by RTO at 2.5V reverse biased.

In Figure 8, the cumulative probability distribution of P-19 junction leakage for all of split conditions show the independence of the junction leakage current of the SAC-OX of Well I/I and S/D I/I by RTO and much more sensitive to that of SAC-OX by FO. In figure 9, the cumulative probability distribution of P-20 junction leakage indicates that the thermal budget of SCA-OX of Well I/I is the key parameters and the lager thickness of SAC-OX of S/D I/I provide more protection to prevent the I/I damage.

Based on the analysis of process monitor test structures of junction leakage, the optimized process is proposed: SAC-OX grown by FO (9.4 nm, 750 ^{0}C) and by RTO (10.0 nm, 1075 ^{0}C), both of SAC-OX of S/D I/I are 18.5 nm post the spacer etching. Figures 10 and 11 show the cumulative probability distribution of N^+/P-Well junction leakage of SRAM Cell-A, and Cell-B. Both of the optimized processes come with the same distribution as the thickness of SAC-OX of S/D I/I is 18.5 nm.

Summary

The impact of SAC-OX of Well and S/D I/I to the N^+/P-Well junction leakage is evaluated for the first time. The potential nucleation source of dislocation at the Poly mask edges is generated by the thermal oxidation of Well I/I sacrificial oxide and the dislocation under the Poly mask edges is dominating the N^+/P-Well junction leakage. The potential nucleation source of dislocation is triggered and formed the dislocation at corner of STI under Poly mask edges. The thicker thickness of SAC-OX of S/D I/I could provide much more resistant to ion implantation damage.

Reference

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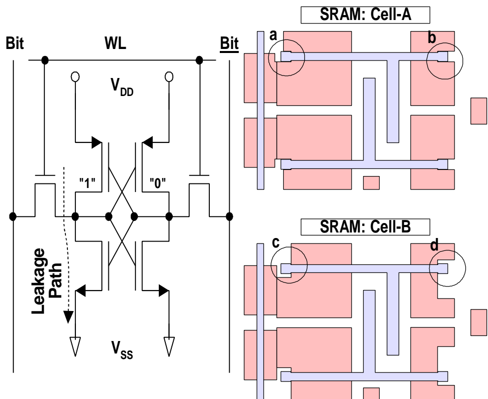


Fig. 1: Leakage path of failed SRAM and schematic layout of SRAM cell-A ,cell-B

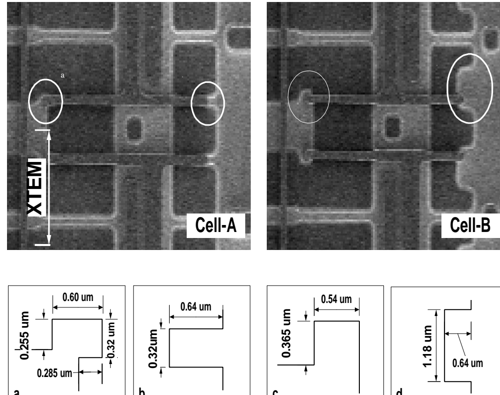


Fig. 2: SEM micorgaphs of SRAM cell-A, and cell-B

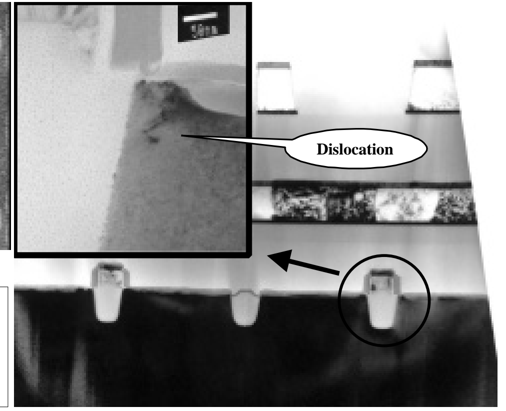
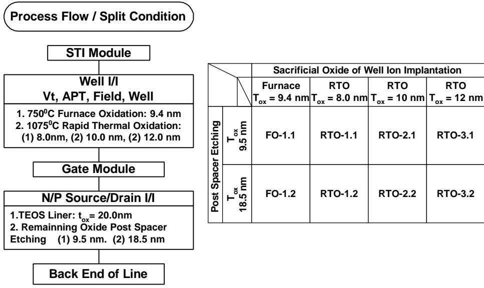


Fig. 3: TEM micorgaphs of failed cell-A.



Process Flow / Split Condition

STI Module

Well I/I
Vt, APT, Field, Well

1. 750°C Furnace Oxidation: 9.4 nm
2. 1075°C Rapid Thermal Oxidation: (1) 8.0nm, (2) 10.0 nm, (2) 12.0 nm

Gate Module

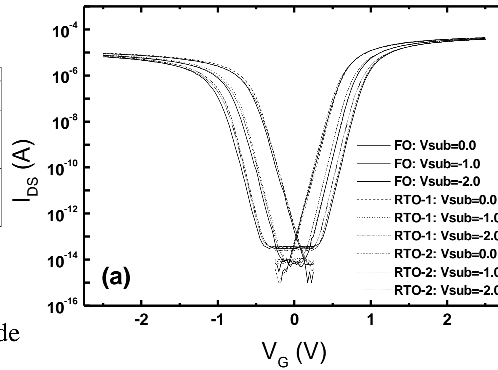
N/P Source/Drain I/I

1.TEOS Liner: t_{ox}= 20.0nm
2. Remainning Oxide Post Spacer Etching (1) 9.5 nm. (2) 18.5 nm

Back End of Line

		Sacrificial Oxide of Well Ion Implantation			
		Furnace T_{ox} = 9.4 nm	RTO T_{ox} = 8.0 nm	RTO T_{ox} = 10 nm	RTO T_{ox} = 12 nm
Post Spacer Etching	T_{ox} 9.5 nm	FO-1.1	RTO-1.1	RTO-2.1	RTO-3.1
	T_{ox} 18.5 nm	FO-1.2	RTO-1.2	RTO-2.2	RTO-3.2

Fig. 4: Schematic process and sacrificial oxide split conditions.



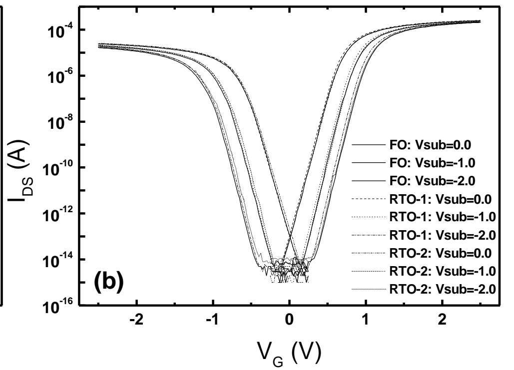


Fig. 5: (a) I_D-V_G of narrow width MOSFETs (W_G/L_G = 0.35/0.25 um). V_D=0.25V (b) I_D-V_G of cell-like MOSFETs. ($W_{NG}/W_{PG}/L_{PG}$ = 2.79/1.0/0.25 um). V_D=0.25V

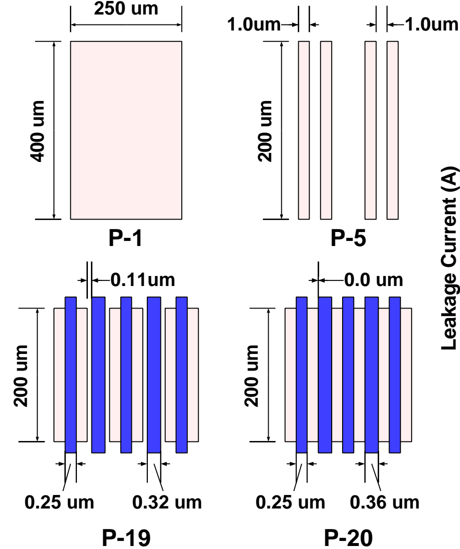


Fig. 6: Schematic layout of test structure of Junction leakage.

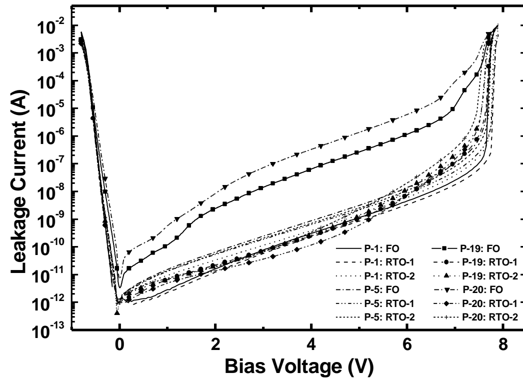


Fig. 7: I-V characteristics of P-1, P-5, P-19, and P-20 N^+/P-Well junction leakage.

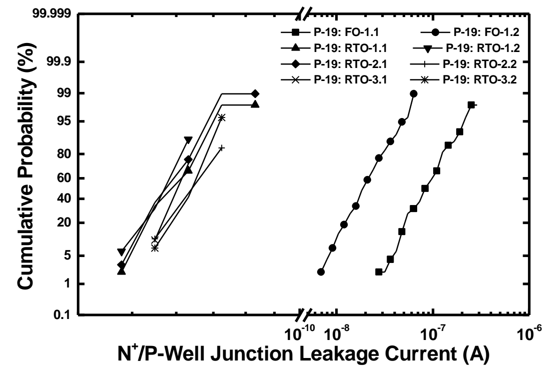


Fig. 8: Cumulative distribution of P-19 N^+/P-Well junction leakage.

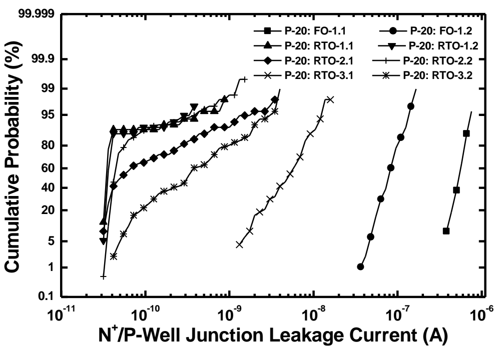


Fig. 9: Cumulative distribution of P-20 N^+/P-Well junction leakage.

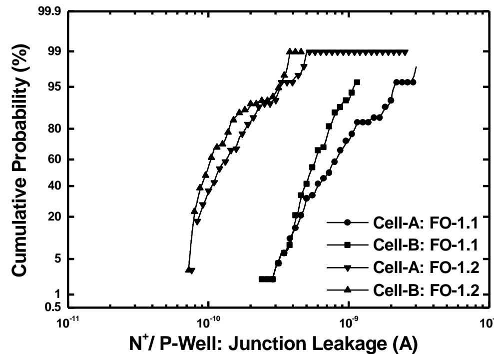


Fig. 10: Cumulative distribution of SRAM cell N^+/P-Well junction leakage. Furnace oxidation: T_{ox} of SAC = 9.7 nm. Post Spacer etching T_{ox} of SAC = 9.5 nm, and 18.5 nm for FO-1.1, and FO-1.2, respectively.

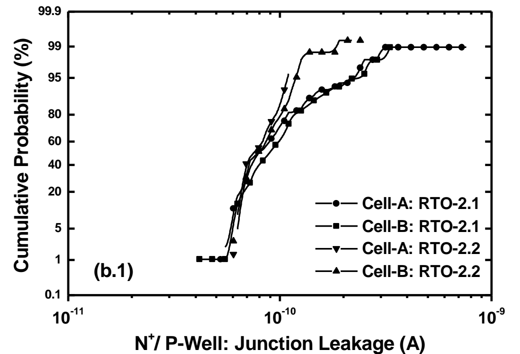


Fig. 11: Cumulative distribution of SRAM Cell N^+/P-Well junction leakage. Furnace oxidation: T_{ox} of SAC = 10.0 nm. Post Spacer etching T_{ox} of SAC = 9.5 nm, and 18.5 nm for RTO-2.1, and RTO-2.2, respectively.