



# MicroConverter™, Multi-Channel 12 bit ADC with Embedded MCU

## Preliminary Technical Data

## ADuC812

### FEATURES

#### ANALOG I/O

- 8 Channel (52 PQFP), true 12 bit ADC
- 6 Channel (44 PLCC), true 12 bit ADC
- Self Calibrating
- High Speed 200 kSPS
- On-chip DMA Controller for auto-capture
- Dual 12-bit Voltage DAC's
- On-chip temperature sensor function

#### MEMORY

- 8K Bytes On-Chip Program Flash EEPROM
- 640 Bytes On-Chip Data Flash EEPROM
- 256 Bytes On-Chip Data RAM
- 16M Bytes Ext. Data Address Space
- 64K Bytes Ext. Program Address Space

#### 8051 BASED CORE

- 8051 Compatible Instruction Set
- 12 MHz Nominal Operation
- Three 16 bit Timer/Counters
- 32 Programmable I/O lines
- Nine interrupt sources, two priority levels

#### POWER

- Specified for 3V and 5V operation
- Normal, Sleep and Powerdown Modes

#### On-Chip PERIPHERALS

- UART Serial I/O
- 2 Wire(I2C® Compatible) and SPI® Serial I/O
- Watchdog Timer
- Power Supply Monitor

### GENERAL DESCRIPTION

The ADuC812 is a fully integrated 12 bit data acquisition system incorporating a high performance self calibrating multi-channel ADC, dual DACs and programmable 8 bit MCU (8051 instruction set compatible) on a single chip. 8K bytes FLASH program memory, 640 bytes FLASH user memory and 256 bytes RAM are also incorporated On-Chip. Program memory security lock features are provided on-chip.

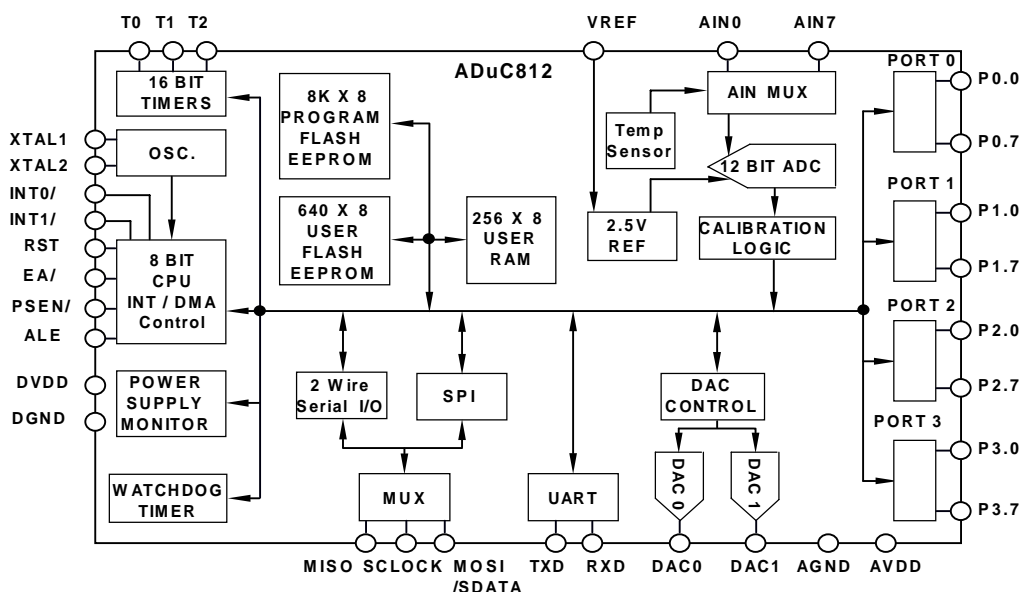
Additional MCU support functions include Watchdog Timer, Power Supply Monitor and ADC DMA functions. 32 Programmable I/O lines, I2C compatible, SPI and Standard UART Serial Port I/O are provided for multi-processor interfaces and I/O expansion.

Static CPU operation, sleep and powerdown modes for the converters allow power management for low power applications. The part is available in 44 pin, plastic lead chip carrier (PLCC) and 52 pin, plastic quad flatpack package (PQFP).

### APPLICATIONS

Intelligent Sensor calibration and conditioning  
Battery Powered Systems (Portable PCs,  
Instruments, Monitors)  
Transient Capture Systems  
DAS and Communications Systems

### FUNCTIONAL BLOCK DIAGRAM



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# ADuC812-SPECIFICATIONS<sup>1, 2</sup>

( $V_{DD}=DV_{DD}=+3.0\text{ V}$  or  $+5.0\text{ V} \pm 10\%$ ,  $REF_{IN}/REF_{OUT} = 2.5\text{V}$  Internal Reference,  $Mclkin = 11.0592\text{MHz}$ ,  $f_{sample} = 200\text{KHz}$ ,  
DAC  $V_{OUT}$  Load to AGND;  $R_L = 10\text{K}\Omega$ ,  $C_L = 100\text{pF}$ . All specifications  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless other wise noted.

Parameter	ADuC812	Units	Test	Conditions/Comments
ADC CHANNEL SPECIFICATIONS				
DC ACCURACY				
Resolution	12	Bits		
Integral Nonlinearity	$\pm 1/2$	LSB		5V Reference, $V_{DD} = 5\text{V}$
Differential Nonlinearity	$\pm 1$	LSB		Guaranteed No Missing Codes to 12 Bits
Offset Error	$\pm 2$	LSB		
Offset Error Match	2	LSB		
Fullscale Error	$\pm 2$	LSB		
Fullscale Error Match	1	LSB		
DYNAMIC PERFORMANCE				
Signal to Noise Ratio (SNR) <sup>3, 4</sup>	70	dB		Typical SNR is 72 dB
Total Harmonic Distortion (THD) <sup>4</sup>	-78	dB		
Peak Harmonic or Spurious Noise <sup>4</sup>	-78	dB		
ANALOG INPUT				
Input Voltage Ranges	0 to $V_{REF}$	Volts		
Leakage Current	$\pm 1$	$\mu\text{A}$ max		
Input Capacitance	20	pF typ		
REFERENCE INPUT/OUTPUT				
$REF_{in}$ Input Voltage Range	$2.3/V_{DD}$	V min/max		
Input Impedance	150	$\text{K}\Omega$		
$REF_{OUT}$ Output Voltage	$2.3/2.7$	V min/max		
$REF_{OUT}$ Tempco	20	ppm/ $^{\circ}\text{C}$ typ		
CONVERSION RATE				
Conversion Time	4.5	$\mu\text{s}$ max		
Track/Hold Acquisition Time	0.5	$\mu\text{s}$ min		
SYSTEM CALIBRATION				
Offset Calibration Span <sup>5</sup>	$+0.05 \text{ X } V_{REF} / -0.05 \text{ X } V_{REF}$	V max/min		Allowable Offset Voltage Span for Calibration
Gain Calibration Span <sup>5</sup>	$1.025 \text{ X } V_{REF} / -0.975 \text{ X } V_{REF}$	V max/min		Allowable Full-Scale Voltage Span for Calibration
DAC CHANNEL SPECIFICATIONS				
DC ACCURACY				
Resolution	12	Bits		
Relative Accuracy	$\pm 2$	LSB max		
Differential Nonlinearity	$\pm 1$	LSB max		
Offset Error	$\pm 50$	mV max		
Fullscale Error	$\pm 100$	mV max		
Fullscale Mismatch	TBD	% of Fullscale on DAC1		
ANALOG OUTPUTS				
Voltage Range	0 to $V_{REF}$ , 0 to $V_{DD}$	Volts		DAC $V_{REF} = 2.5\text{V}$
Resistive Load	10	$\text{K}\Omega$ typ		
Capacitive Load	50	pF typ		
Output Impedance	TBD	$\Omega$ typ		
I sink	50	$\mu\text{A}$ typ		

# Preliminary Technical Data

# ADuC812

Parameter	ADuC812	Units	Test Conditions/Comments
DAC AC CHARACTERISTICS			
Voltage Output Settling Time	4	us typ	Fullscale Settling Time to Within 1/2LSB of Final Value
Digital-to-Analog Glitch Energy	TBD	nVsec typ	DAC Code Changes All 1's to All 0's
FLASH MEMORY RELIABILITY CHARACTERISTICS			
Endurance	1000, 10,000	Cycles	Method TBD
Data Retention	100	Years	Method TBD
WATCHDOG TIMER CHARACTERISTICS			
Oscillator frequency	64	kHz typ	
Oscillator frequency tolerance	$\pm 25$	% max	
POWER SUPPLY MONITOR CHARACTERISTICS			
Power supply trip point accuracy	$\pm 2.5$	% of selected trip point typ	Applicable to all 5 user selectable trip points
DIGITAL INPUTS			
Input high Voltage (V <sub>inh</sub> )	2.4	V min	V <sub>DD</sub> = 4.5V to 5.5V
	2.1	V min	V <sub>DD</sub> = 2.7V to 3.3V
Input Low Voltage (V <sub>inl</sub> )	0.8	V max	V <sub>DD</sub> = 4.5V to 5.5V
	0.6	V max	V <sub>DD</sub> = 2.7V to 3.3V
Input Current (I <sub>in</sub> )	$\pm 10$	uA max	V <sub>in</sub> = 0V or V <sub>DD</sub>
Input Capacitance <sup>6</sup>	10	pF typ	
DIGITAL OUTPUTS			
Output High Voltage (V <sub>oh</sub> )	4.0	Vmin	V <sub>DD</sub> = 4.5V to 5.5V
	2.4	Vmin	V <sub>DD</sub> = 2.7V to 3.3V
Output Low Voltage (V <sub>ol</sub> )	0.4	V max	Is <sub>source</sub> = 200uA
Floating State Leakage Current	$\pm 10$	uA max	Is <sub>sink</sub> = 1.6mA
Floating State Output Capacitance <sup>6</sup>	10	pF typ	
POWER REQUIREMENTS			
I <sub>dd</sub> Active	TBD	mA max	V <sub>DD</sub> = 4.5V to 5.5V
	TBD	mA max	V <sub>DD</sub> = 2.7V to 3.3V
I <sub>dd</sub> Idle	TBD	mA max	V <sub>DD</sub> = 4.5V to 5.5V
	TBD	mA max	V <sub>DD</sub> = 2.7V to 3.3V
I <sub>dd</sub> Powerdown	TBD	uA max	TBD

## NOTES

<sup>1</sup> Specifications apply after calibration.

<sup>2</sup> Temperature Range -40°C to +85°C.

<sup>3</sup> SNR calculation includes distortion and noise components.

<sup>4</sup> Measured with V<sub>in</sub> = 10 kHz Sine Wave, f<sub>SAMPLE</sub> = 200 kHz.

<sup>5</sup> The offset and gain calibration spans are defined as the range of offset and gain errors that the ADuC812 can calibrate.

<sup>6</sup> Not production tested, guaranteed by characterisation at initial product release.

Specifications subject to change without notice.

# Preliminary Technical Data

# ADuC812

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to GND	-0.3V to +7V
Digital Input Voltage to GND (CONVST, SCLK)	-0.3V, V <sub>DD</sub> + 0.3V
Digital Output Voltage to GND (D <sub>OUT</sub> )	-0.3V, V <sub>DD</sub> + 0.3V
V <sub>REF</sub> to GND	-0.3V, V <sub>DD</sub> + 0.3V
Analog Inputs (V <sub>IN+</sub> , V <sub>IN-</sub> )	-0.3V, V <sub>DD</sub> + 0.3V
Storage Temperature Range	-65°C to 150°C
Junction Temperature	+150°C

<sup>1</sup> Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Plastic LCC Package, Power Dissipation	TBD
θ <sub>JA</sub> Thermal Impedance	TBD
θ <sub>JC</sub> Thermal Impedance	TBD
PQFP Package, Power Dissipation	TBD
θ <sub>JA</sub> Thermal Impedance	TBD
θ <sub>JC</sub> Thermal Impedance	TBD
Lead Temperature, Soldering	
Vapor Phase (60sec)	TBD
Infrared (15 sec)	TBD

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7823 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## TERMINOLOGY

### ADC SPECIFICATIONS

#### Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition and full scale, a point 1/2 LSB above the last code transition.

#### Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

#### Offset Error

This is the deviation of the first code transition (0000...000) to (0000...001) from the ideal, i.e. +1/2 LSB

#### Full Scale Error

This is the deviation of the last code transition from the ideal A<sub>in</sub> voltage (Full Scale - 1.5 LSB) after the offset error has been adjusted out.

#### Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency (f<sub>s</sub>/2), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02N + 1.76) \text{ dB}$$

Thus for a 12-bit converter, this is 74 dB

#### Total Harmonic Distortion

Total Harmonic Distortion is the ratio of the rms sum of the harmonics to the fundamental.

### DAC SPECIFICATIONS

#### Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

#### Voltage Output Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

#### Digital to Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nVsec.

## ADuC812 ARCHITECTURE, MAIN FEATURES

The ADuC812 is a highly integrated true 12-bit data acquisition system. At its core, the ADuC812 incorporates a high performance 8 bit MCU (8051 Instruction Set Compatible) with on-chip reprogrammable non-volatile Flash program memory controlling a multi-channel (8 input channels on 52PQFP and 6 channels on 44PLCC), true 12-bit ADC.

The chip incorporates all secondary functions to fully support the programmable data acquisition core. These secondary functions include User data Flash memory, Watchdog Timer (WDT), Power Supply Monitor (PSM) and various industry standard parallel and serial interfaces.

## ADuC812 MEMORY ORGANISATION

As with all 8051 related devices, the ADuC812 has separate address spaces for Program and Data memory as shown in Figure 1. As shown in Figure 1, an additional 640 Bytes of Flash EEPROM are also available to the user and are accessed indirectly via a group of control registers mapped in the Special Function Register (SFR) area in the Data Memory Space.

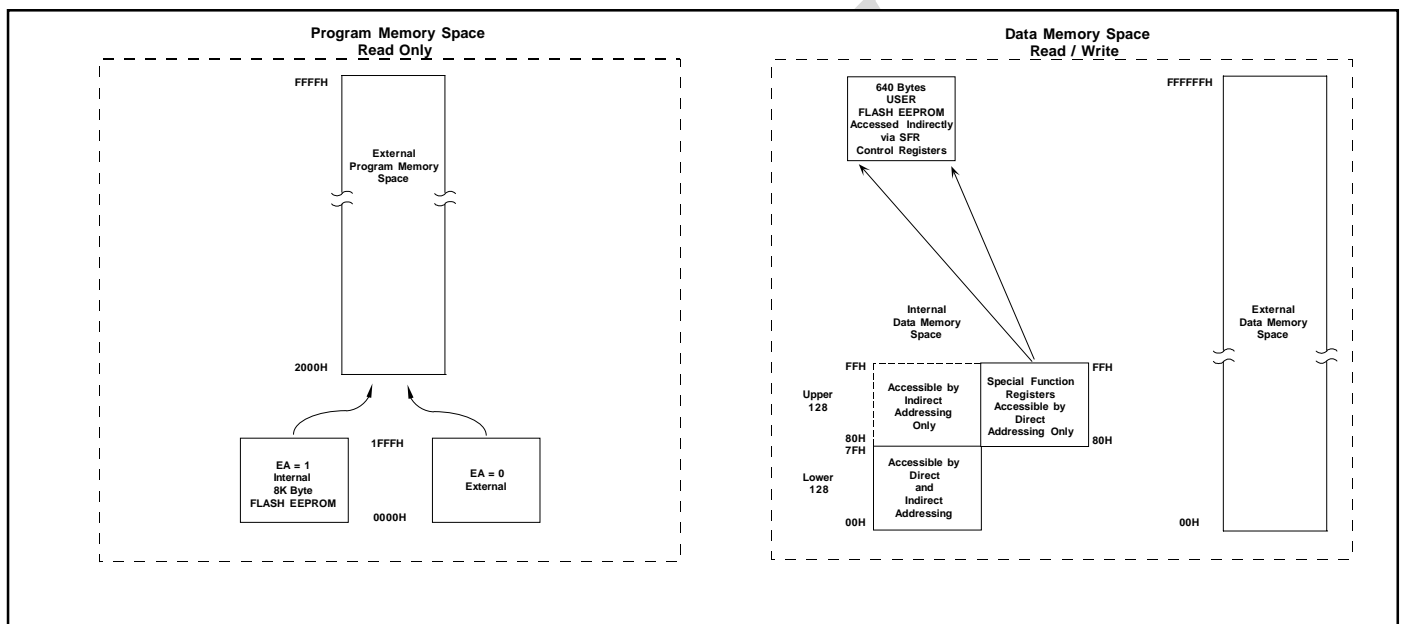


Figure 1. ADuC812 Program and Data Memory Maps

The lower 128 bytes of internal data memory are mapped as shown in Figure 2. The lowest 32 bytes are grouped into 4 banks of 8 registers addressed as R0 through R7. The next 16 bytes (128 bits) above the register banks form a block of bit addressable memory space at bit addresses 00H through 7FH.

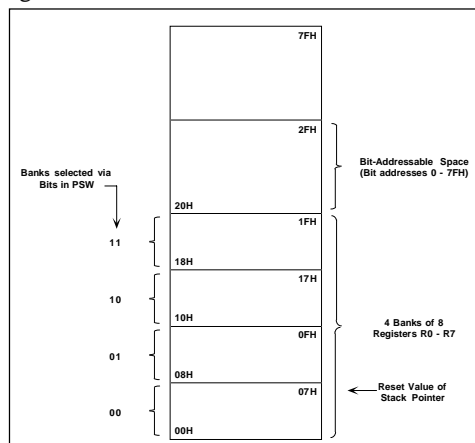


Figure 2. Lower 128 Bytes of Internal RAM

The SFR space is mapped in the upper 128 bytes of internal data memory space. The SFR area is accessed by direct addressing only and provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC812 via the SFR area is shown in Figure 3.

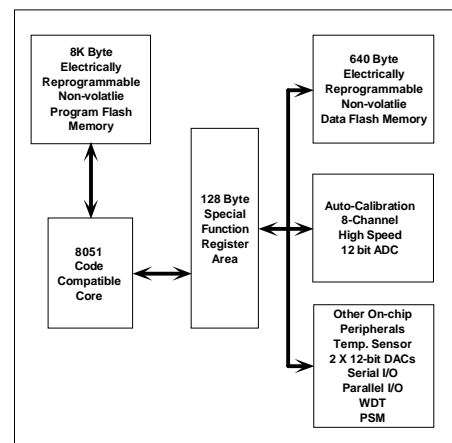


Figure 3. ADuC812 Programming Model.

## CORE CPU OPERATION

At the heart of the ADuC812 is an 8052 instruction compatible CPU. An on-chip oscillator is used as the clock source for the CPU to which all operations are synchronised. The on-chip oscillator is driven by connecting an external crystal to the XTAL1 and XTAL2 pins on the device. A typical ADuC812 machine cycle is shown in Figure 5. The machine cycle consists of a sequence of 6 states, numbered S1 through S6. Each state last for two oscillator periods, P1, P2. Thus a machine cycle takes 12 oscillator periods or 1µs if the oscillator frequency is 12MHz.

In applications that will use the UART serial port as the main communications link to the MicroConverter, a master oscillator frequency of 11.0592MHz. is used yielding a machine cycle rate of 921.6 KHz. This seemingly odd cycle rate is easily divided using on-chip timers to generate standard comms baud rates e.g.. 19200, 9600 baud etc.

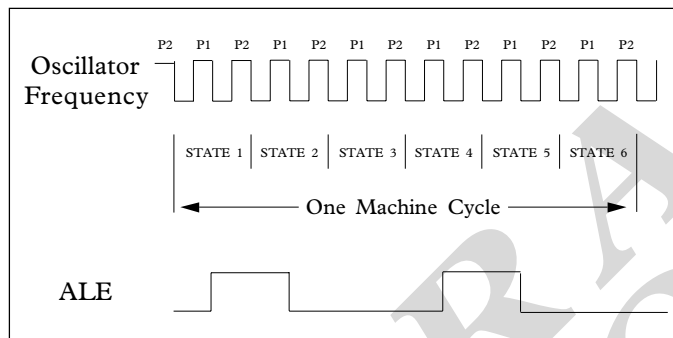


Figure 5. ADuC812 Machine Cycle Timing

## Overview of CPU Related SFRs

### Accumulator

ACC is the Accumulator register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for Accumulator specific instructions refer to the Accumulator as A.

### B Register

The B register is used with the ACC for multiplication and division operations. For other instructions it can be treated as a general purpose scratchpad register.

### Stack Pointer

The SP register is the stack pointer and is used to hold an internal RAM address that is called the 'top of the stack'. The SP register is incremented before data is stored during PUSH and CALL executions. While the Stack may reside anywhere in on-chip RAM, the SP register is initialized to 07 after a reset. This causes the stack to begin at location 08H.

## Data Pointer

The DPTR register is the Data Pointer and is made up of three 8 bit registers, named DPP (page byte), DPH (high byte) and DPL (low byte). These are used to provide memory addresses for internal and external code access and external data access. It may be manipulated as a 24 bit register (DPTR) or as three independent 8 bit registers (DPP, DPH, DPL).

## Program Status Word

The PSW register is the Program Status Word which contains several bits reflecting the current state of the CPU as detailed in Figure 6.

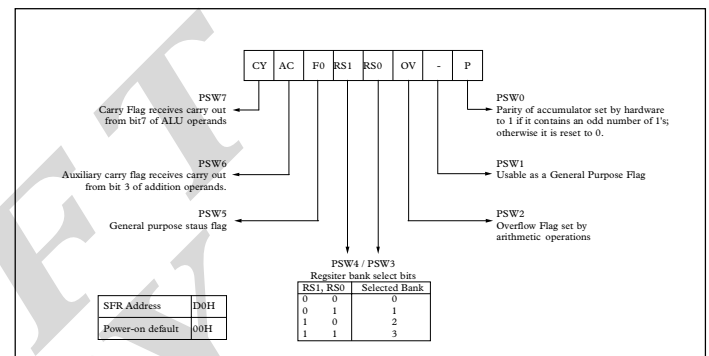


Figure 6. PSW SFR bit designations

## Power Control

The Power Control (PCON) register contains bits for power saving options and general purpose status flags as shown in figure 7. It should be noted that in idle mode the clock signal is gated off to the CPU but not to the Interrupt, Timer and Serial Port logic. All registers maintain their data during idle. Idle mode can be terminated by activation of an enabled interrupt or a valid reset signal at the external Reset pin.

In Power-Down mode, the clock signal is gated off to the all functions on the chip and can only be disabled with a valid reset signal on the external Reset pin.

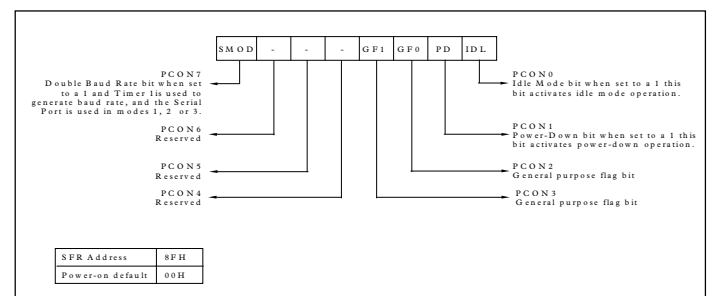


Figure 7. PCON SFR bit designations

## Power-on Reset

An on-chip, power-on reset circuit guarantees a valid internal reset signal is generated when the power supply is connected to the device. This ensures all on-chip components are powered on in a valid default configuration. The power-on reset circuit does not require any external components.

## ADC CIRCUIT INFORMATION

### General Overview

The ADC conversion block incorporates a fast, multi-channel, 12-bit, single supply A/D converter. This block provides the user with multi-channel mux, track/hold, on-chip reference, calibration features and A/D converter. All components in this block are easily configured via the SFR interface from the core MCU.

The A/D converter section in this block consists of a conventional successive-approximation converter based around a capacitor DAC. The converter accepts an analog input range of 0 to  $+V_{REF}$ . A high precision, low drift 2.5V reference is provided on-chip. The internal reference may be overdriven via the external  $V_{REF}$  pin. This external reference can be in the range 2.3V to  $AV_{DD}$ .

Single step or continuous conversion modes can be initiated in software or alternatively by applying a convert signal to the an external pin. Timer 2 can also be configured to generate a repetitive trigger for ADC conversions. The ADC may also be configured to operate in a DMA Mode whereby the ADC block continuously converts and captures samples without any interaction from the MCU core.

The ADC core contains self-calibration and system calibration options to ensure accurate operation over time and temperature. A voltage output from an On-Chip bandgap reference proportional to absolute temperature can also be routed through the front-end ADC multiplexor facilitating a temperature sensor implementation.

### Transfer Function

The analog input range for the ADC is 0 V to  $V_{REF}$ . For this range, the designed code transitions occur mid-way between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS - 3/2 LSBs). The output coding is straight binary with 1 LSB = FS/4096 or 2.5 V/4096 = 0.61 mV when  $V_{REF}$  = 2.5 V. The ideal input/output transfer characteristic for the 0 to  $V_{REF}$  range is shown in Figure 8.

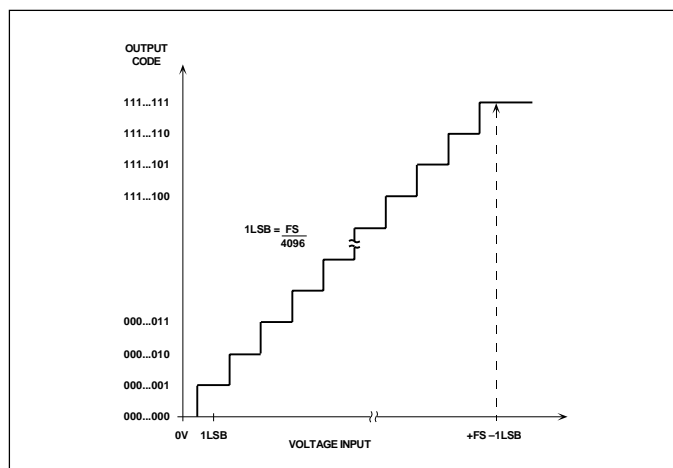


Figure 8. ADuC812 ADC Transfer Function

### SFR Interface to ADC Block

The ADC operation is fully controlled via 3 SFR's, namely :

- ADCCON1** - Controls acquisition and conversion times and powerdown modes as detailed in Figure 9.

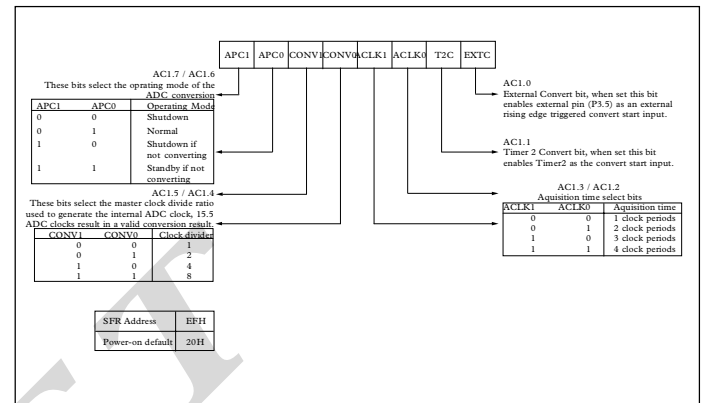


Figure 9. ADCCON1 SFR bit designations

- ADCCON2** - Controls channel selection and conversion modes as detailed in Figure 10.

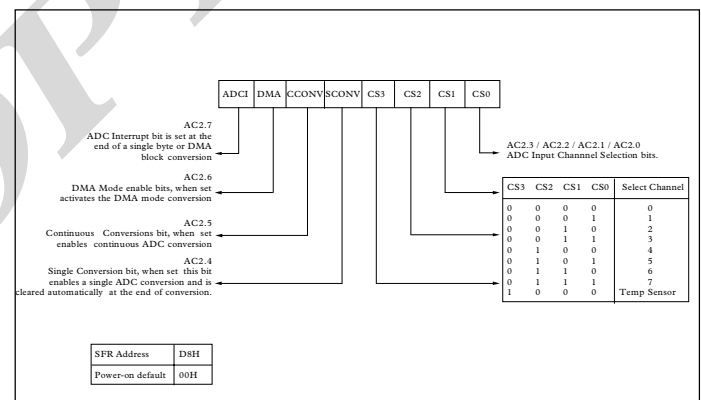


Figure 10. ADCCON2 SFR bit designations

- ADCCON3** - Controls user calibration options and Busy status as detailed in Figure 11.

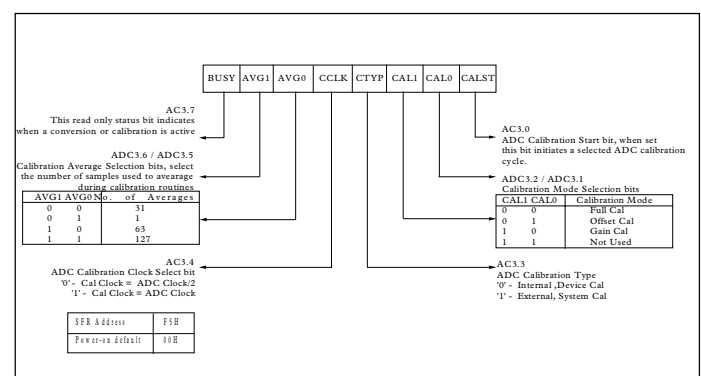


Figure 11. ADCCON3 SFR bit designations