RS

Data Sheet

Microprocessor compatible real time clock IC 146818

RS stock number 302-003

The 146818 is a 6800 peripheral CMOS device which combines three unique features: a complete time-of-day clock with alarm, calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of Low-power static RAM.

This device includes 6800 multiplexed bus interface circuit and 8085s multiplexed bus interface as well, so it can be directly connected to 8085 etc.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS part including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the 146818 may be used with a CMOS microprocessor to relieve the software of time-keeping work-load and to extend the available RAM of an MPU.
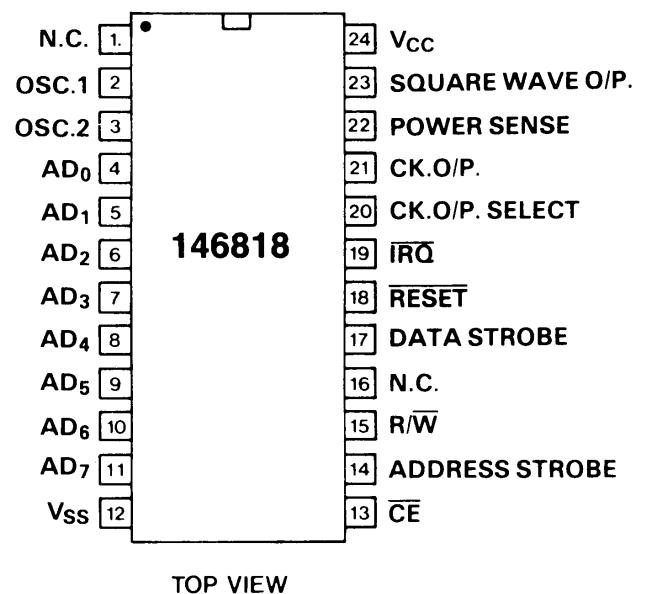
● Three Interrupts are Separately Software Maskable and Testable
 • Time-of-Day Alarm, Once-per-Second to Once-per-Day
 • Periodic Rates from 30.5µs to 500ms
 • End-of-Clock Update Cycle
● Programmable Square-Wave Output Signal
● Three Time Base Input Options
 • 4.194304MHz
 • 1.048576MHz
 • 32.768kHz
● Clock Output may be used as Microprocessor Clock Input
 • At Time Base Frequency ÷ 4 or ÷ 1
● Multiplexed Bus Interface Circuit
● Low-Power, High-Speed, High-Density CMOS.

Absolute maximum ratings

Supply voltage V_{CC} _____ -0.3 to +7.0V
Input voltage _____ -0.3 to +7.0V
Operating temperature range _____ 0 to 70°C
Storage temperature range _____ -55 to +150°C

Features

● Time-of-Day Clock and Calendar
 • Counts Seconds, Minutes, and Hours of the Day
 • Counts Days of Week, Date, Month, and Year
● Binary or BCD Representation of Time, Calendar, and Alarm
● 12- or 24 Hour Clock with AM and PM in 12-Hour Mode
● Automatic End of Month Recognition
● Automatic Leap Year Compensation
● Interfaced with Software as 64 RAM Locations
 • 14 Bytes of Clock and Control Register
 • 50 Bytes of General Purpose RAM

Pin	Signal	Pin	Signal
1	N.C.	24	V_{CC}
2	OSC.1	23	SQUARE WAVE O/P.
3	OSC.2	22	POWER SENSE
4	AD_0	21	CK.O/P.
5	AD_1	20	CK.O/P. SELECT
6	AD_2	19	$\overline{IRQ}$
7	AD_3	18	$\overline{RESET}$
8	AD_4	17	DATA STROBE
9	AD_5	16	N.C.
10	AD_6	15	$R/\overline{W}$
11	AD_7	14	ADDRESS STROBE
12	V_{SS}	13	$\overline{CE}$

146818

TOP VIEW

Electrical characteristics dc (V_{CC} = 5.0V ± 10%, V_{SS} = 0V, Ta = 0 to + 70°C, unless otherwise noted.)

Parameter		Symbol	Test Condition	min.	typ.	max.	Unit
Supply voltage	V_{CC}			4.5	5.0	5.5	V
Input voltage	V_{IL}			-0.3	-	0.7	V
	V_{IH}			V_{CC}-1.0	-	V_{CC}	V
Operating temperature	T_{opr}			0	25	70	°C
Input "High" voltage	$AD_0 \sim AD_7$, $\overline{CE}$, AS, $R/\overline{W}$, DS, CKFS, PS	V_{IH}		V_{CC}-2.0	-	V_{CC}	V
	$\overline{RES}$			V_{CC}-1.0	-	V_{CC}	
	OSC_1			V_{CC}-1.0	-	V_{CC}	

* The time base frequency to be used needs to be chosen in Register A.

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Input "Low" voltage	$AD_0 \sim AD_7$, $\overline{CE}$, AS, R/W, DS, CKFS, PS	V_{IL}		-0.3	-	0.7	V
	$\overline{RES}$			-0.3	-	0.8	
	OSC1			-0.3	-	0.8	
Input Leakage Current	OSC1, $\overline{CE}$, AS, R/W, DS, $\overline{RES}$, CKFS, PS	$|I_{in}|$		-	-	2.5	μA
Three-state (off state) Input Current	$AD_0 \sim AD_7$	$|I_{TSI}|$		-	-	10	μA
Output Leakage Current	$\overline{IRQ}$	I_{LOH}		-	-	10	μA
Output "High" Voltage	$AD_0 \sim AD_7$ / SQW, CKOUT	V_{OH}	$I_{OH} = -1.6mA$	4.1	-	-	V
	$AD_0 \sim AD_7$ / SOW, CKOUT		$I_{OH} < -10$ μA	VCC-0.1	-	-	
Output 'Low" Voltage	$AD_0 \sim AD_7$	V_{OL}	$I_{OL} = 1.6mA$	-	-	0.5	V
	CKOUT		$I_{OL} = 1.6mA$				
	$\overline{IRQ}$, SQW		$I_{OL} = 1.6mA$				
Input Capacitance	$AD_0 \sim AD_7$	C_{IN}	$V_{IN} = 0V$	-	-	12.5	pF
	All inputs except $AD_0 \sim AD_7$		$Ta = 25°C$ / $f = 1$ MHz	-	-	12.5	
Output Capacitance	SQW, CKOUT, $\overline{IRQ}$	C_{out}		-	-	12.5	
Supply Current (MPU Read/ Write operating)	Crystal Oscillation	$f_{OSC} = 4MHz$	$V_{CC} = 5.0V$ SQW: disable CKOUT = fOSC (No Load) $t_{CVC} = 1$ μs Circuit: Fig. 10 Parameter: Table 1	-	-	10	mA
		$f_{OSC} = 1MHz$		-	-	7	
		$f_{OSC} = 32kHz$		-	-	5	
Supply Current (MPU not operating)		$f_{OSC} = 4MHz$	$I_{CC}*$	-	-	5	
		$f_{OSC} = 1MHz$		-	-	2	
		$f_{OSC} = 32kHz$		-	300	500	μA
Supply Current (MPU Read/ Write Operating)	External Clock	$f_{OSC} = 4MHz$	$V_{CC} = 5.0V$ SQW: disable CKOUT = fOSC (No Load) OSC_2: open $t_{CVC} = 1$ μs Circuit: Fig. 15	-	-	10	mA
		$f_{OSC} = 1MHz$		-	-	7	
		$f_{OSC} = 32kHz$		-	-	5	
Supply Current (MPU not operating)		$f_{OSC} = 4MHz$	$I_{CC}*$	-	-	4	
		$f_{OSC} = 1MHz$		-	-	1	
		$f_{OSC} = 32kHz$		-	60	100	μA

Electrical characteristics

Low voltage standby operation

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Supply voltage	V_{CCL}		2.7		4.5	V
Supply current	I_{CCL}	$V_{CCL} = 3.0V$ SQW disabled CK OUT = f_{OSC}				
		XTAL 4MHz			600	μA
		XTAL 1MHz			350	μA
		XTAL 32kHz		50	100	μA
		EXTERNAL 4MHz			500	μA
		EXTERNAL 1MHz			150	μA
		EXTERNAL 32kHz		30	70	μA
Set up time to low voltage operation	t_{CE}		0			ns
Set up time to normal voltage operation	t_r		t_{cyc}(953)			ns
Fall time of V_{CC}	t_{pf}		300			μs
Rise time of V_{CC}	t_{pr}		300			μs
Input high level $\overline{CE}$, CKFS	V_{ihL}	$V_{CC}L = 2.7$ to $3.5V$	$0.7 \times V_{CC}L$		$V_{CC}L$	V
PS		$V_{CC}L = 3.5$ to $4.5V$	2.5		$V_{CC}L$	V
Input high level $\overline{RES}$			$0.8 \times V_{CC}L$		$V_{CC}L$	V
Input high level OSC1			$0.8 \times V_{CC}L$		$V_{CC}L$	V
Input low level CKFS, PS	V_{iLL}		-0.3		0.5	V
$\overline{RES}$			-0.3		0.5	V
OSC1			-0.3		0.5	V
Output high level	V_{ohL}	$I_{OH} = -800$μA/	$-0.8 \times V_{CC}$			
Output low level	V_{oLL}	$I_{OL} = -800$μA/			0.5	V
SQW, CK, $\overline{IRQ}$						

AC CHARACTERISTICS ($V_{CC} = 5.,0V \pm 10\%$, $V_{SS} - 0V$, $T_a = 0 \sim +70°C$, unless otherwise noted)

Bus Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Cycle Time	t_{cyc}	953	-	-	ns
Pulse Width, AAS/ALE 'High"	PW_{ASH}	100	-	-	ns
AS Rise Time	t_{ASr}	-	-	30	ns
AS Fall Time	t_{ASf}	-	-	30	ns
Delay Time DS/E to AS/ALE Rise	t_{ASD}	40	-	-	ns
DS Rise Time	t_{DSr}	-	-	30	ns
DS Fall Time	t_{DSf}	-	-	30	ns
Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ "High"	PW_{DSH}	325	-	-	ns
Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ "Low"	PW_{DSL}	300	-	-	ns
Delay Time, AS/ALE to DS/E Rise	t_{ASDS}	90	-	-	ns
Address Setup Time (R/W)	t_{AS1}	15	-	-	ns
Address Setup Time (CE)	T_{AS2}	55	-	-	ns
Address Hold Time (R/W, $\overline{CE}$)	t_{AH}	10	-	-	ns
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	50	-	-	NS
Muxed Address Hold Time	t_{AHL}	20	-	-	ns
Peripheral Data Setup Time	t_{DSW}	195	-	-	ns
Write Data Hold Time	T_{DHW}	0	-	-	ns
Peripheral Output Data Delay Time from DS/E or $\overline{RD}$	t_{DDR}	-	-	220	ns
Read Data Hold Time	t_{DHR}	10	-	-	ns

Control Signal Timing

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Oscillator Startup	1 MHz, 4 MHz		–	–	100	ms
	32 kHz–	t_{RC}	–	–	1000	
Reset Pulse Width		t_{RWL}	5.0	–	–	μs
Reset Delay Time		t_{RLH}	5.0	–	–	μs
Power Sense Pulse Width		t_{PW1}	5.0	–	–	μs
Power Sense Delay Time		t_{PLH}	5.0	–	–	μs
$\overline{IRQ}$ Release from DS		t_{IRDS}	–	–	2.0	μs
$\overline{IRQ}$ Release from $\overline{RES}$		t_{IRR}	–	–	2.0	μs
VRT Bit Delay		t_{VRTD}	–	–	2.0	μs

Figure 1 Bus read, write timing (6800 family)

(NOTE) $V_{IH} = V_{OH} = V_{CC} - 2.0V$
$V_{IL} = 0.7V$
$V_{OL} = 0.5V$

Figure 2 Road timing (8085 family)

(NOTE) $V_{IH} = V_{OH} = V_{CC} - 2.0V$
$V_{IL} = 0.7V$, $V_{OL} = 0.5V$

Figure 3 Write timing (8085 family)

(NOTE) $V_{IH} = V_{CC} - 2.0V$
$V_{IL} = 0.7V$

Figure 4 $\overline{IRQ}$ Release Delay (from DS)

Figure 5 $\overline{IRQ}$ Release Delay (from $\overline{RES}$)

(NOTE) $V_{IL} = 0.7V$, $V_{OH} = V_{CC} - 2.0V$

(NOTE) $V_{IL} = 0.8V$
$V_{OH} = V_{CC} - 2.0V$

Figure 6 VRT Bit Clear Timing

(NOTE) $V_{IH} = V_{CC} - 2.0V$
$V_{IL} = 0.7V$

* The VRT bit is set to a "1" by reading control register #D. There is no additional way to clear the VRT bit.

Figure 7 $\overline{RES}$ Release Delay

(NOTE) $V_{IH} = V_{CC} - 1.0V$

Figure 8 Test Load

C = 130pF
R_L = 2kΩ
R = 2.55kΩ

(a) $AD_0 \sim AD_7$, SQW, CKOUT

(b) $\overline{IRQ}$ Load Circuit

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Figure 9 **Block Diagram**

Crystal Oscillation Circuit

The on-chip oscillator is designed for a parallel resonant crystal at 4.194304 MHz or 1.048576MHz or 32.768kHz frequencies. The crystal connections are shown in Figure 10.

Figure 10 **Crystal Oscillator Connection**
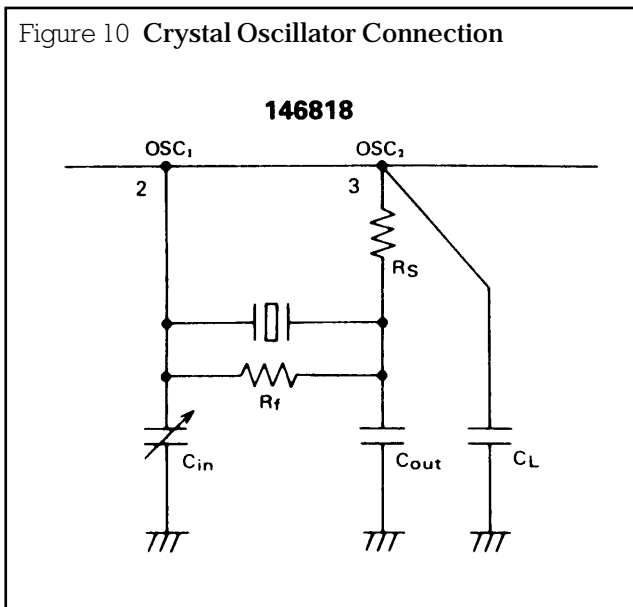
Note: For Board Design of the Oscillation Circuit

In designing the board, the following notes should be taken when the crystal oscillator is used.

1. Crystal oscillator, load capacity C_{in}, C_{out}, C_L and R_f, R_S must be placed as near to the 146818 as possible.

    (Normal oscillation may be disturbed when external noise is induced to pin 2 and 3.)

2. Pin 3 signal line should be wired apart from pin 4 signal line as much as possible. Don't wire them in parallel, or normal oscillation may be disturbed when this signal is fed back to OSC_1.

3. A signal line or a power source line must not cross or go near the oscillation circuit line as shown in the right figure to prevent the induction from these lines and perform the correct oscillation. The resistance between OSC_1, OSC_2 and other pins should be over 10MΩ.

Figure 11 **Note for Board Design of the Oscillation Circuit**
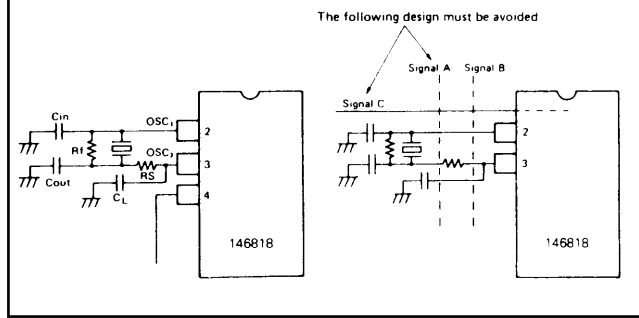
Table 1 **Oscillator Circuit Parameters**

f_{oSC} Parameter	4.194304 MHz	1.048576MHz	32.768kHz
R_S	–	–	150kΩ
R_f	150kΩ	150kΩ	5.6MΩ
C_{in}	22pF	33pF	15pF
C_{out}	22pF	33pF	33pF
C_L	–	–	33pF
CI	80Ω (max.)	700Ω (max.)	40kΩ (max.)

Note: 1. R_S, C_L are used for 32.768 kHz only.
2. Capacitance (C_{in}) should be adjusted to accurate frequency. Parameters listed above are applied to the supply current measurement (see table of DC CHARACTERISTICS).
3. CI: Crystal Impedance.

Interface Circuit for Processors 6800, 8085 etc.

The 146818 has a new interface circuit which permits the 146818 to be directly interfaced with many type of multiplexed bus microprocessors such as 6800 and 8085 etc.

Figure 12 shows the bus control circuit. This circuit automatically selects the processor type by using AS/ASE to latch the state of DS/$\overline{RD}$ pin. Since DS is always "Low" and $\overline{RD}$ is always "High" during AS/ALE, the latch automatically indicates which processor type is connected.

Figure 12 **Functional Diagram of the Bus Control Circuit**
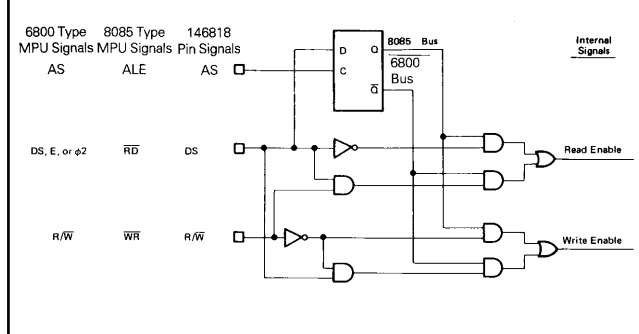
Address Map

Figure 13 shows the address map of the 146818. The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writable by the processor program except

Register C and D which are read only. Bit 7 of Register A and the seconds byte are also read only. Bit 7, of the second byte, always reads "0". The contents of the four control and status registers are described in the Register section.

Time, Calendar and Alarm Locations

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialise the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm byte may be either binary or binary-coded decimal (BCD).

Before initialising the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initialises the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates in the selected data mode. The data mode cannot be changed without reinitialising the 10 data bytes.
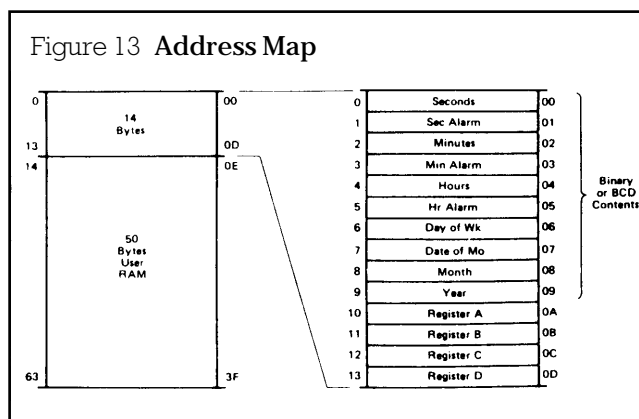
Table 2 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitialising the hour locations. When the 12-hour format is selected the high-order of the hours byte represents PM when it is a "1".

The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced b y one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248 μs at the 4.194304MHz and 1.048567MHz time bases and 1948 μs for the 32.768kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

The three alarm bytes may be used in two ways. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specific time each day if the alarm enable bit is "1". The alternate usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from C0 to FF. That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Figure 13 **Address Map**

Table 2 **Time, Calendar, and Alarm Data Modes**

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0~59	$00~$3B	$00~$59	15	21
1	Seconds Alarm	0~59	$00~$3B	$00~$59	15	21
2	Minutes	0~59	$00~$3B	$00~$59	3A	58
3	Minutes Alarm	0~59	$00~$3B	$00~$59	3A	58
4	Hours (12 Hour Mode)	1~12	$01 ~ $0C (AM) and $81 ~$8C (PM)	$01~$12 (AM) and $81~$92 (PM)	05	05
	Hours (24 Hour Mode)	0~23	$00~$17	$00~$23	05	05
5	Hours Alarm (12 Hour Mode)	1~12	$01~$0C (AM) and $81~$8C (PM)	$01~$12 (AM) and $81~$92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0~23	$00~$17	$00~$23	05	05
6	Day of the Week Sunday = 1	1~7	$01~$07	$01~$07	05	05
7	Day of the Month	1~31	$01~$1F	$01~$31	0F	15
8	Month	1~12	$01~$0C	$01~$12	02	02
9	Year	0~99	$00~$63	$00~$99	4F	79

*Example: 5:58:21 Thursday 15th February 1979

Static CMOS RAM

The 50 general purpose RAM bytes are not dedicated within the 146818. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when main power is removed. The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

The time/calendar functions may be disabled by holding the dividers, in Register A, in the reset state by setting the SET bit in Register B or by removing the oscillator. Holding the dividers in reset prevents interrupts or SQW output from operating while setting the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 59 bytes. Bit 7 of Register A, Registers C and D, and the high-order Bit of the seconds byte cannot effectively be used as general purpose RAM.

Interrupts

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 µs. The update-ended interrupt may be used to indicate to the program that an up-date cycle is completed. Each of these independent interrupt conditions is described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the IRQ pin is immediately activated, though the interrupt indicating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held until after the read cycle. One, two, or three flag bits may be found to be set when Register C is read. The program should inspect all utilised flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt-flag is set and the corresponding interrupt-enable bit is also set, the IRQ pin is asserted "Low". IRQ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a "1" whenever the IRQ pin is being driven "Low".

The processor program can determine that the RTC initiated the interrupt by reading Register C. A "1" in bit 7 (IRQF bit) indicates that one of more interrupts have been initiated by the part. The act of reading Register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set. Again, more than one interrupt-flag bit may be set.

DIVIDER STAGES

The 146818 has 22 binary-divider stages following the time base as shown in Figure 9. The output of the dividers is a 1Hz signal to the update-cycle logic. The dividers are controlled by three divider bits (DV2, DV1, and DV0) in Register A.

Divider Control

The divider-control bits have three uses, as shown in Table 3. Three usable operating time bases may be selected (4.194304MHz, 1.048576MHz, or 32.768kHz). The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one second later. The divider-control bits are also used to facilitate testing the 146818.

Table 3 **Divider Configurations**

Time Base Frequency	Divider Bits Register A			Operation Mode	Divider Reset	Bypass First N-Divider Bits
	DV2	DV1	DV0			
4.194304MHz	0	0	0	Yes	-	N = 0
1.048576MHz	0	0	1	Yes	-	N = 2
32.768kHz	0	1	0	Yes	-	N = 7
Any	1	1	0	No	Yes	-
Any	1	1	1	No	Yes	-

Note: Other combinations of divider bits are used for test purposes only.

Square-Wave Output Selection

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 9. The first purpose of selecting a divider tap is to generate a square-wave output signal in the SQW pin. Four bits in Register A establish the square-wave frequency as listed in Table 4. The SQW frequency selection shares the 1-of-15 selector with periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave enable (SQWE) bit in Register B. Altering the divider, square-wave output selection bits, or the SQW output-enable bit may generate an asymmetrical waveform at the time of execution. The square-wave output pin has a number of potential uses. For example, it can serve as a frequency standard for external use, a frequency synthesiser, or could be used to generate one or more audio tones under program control.

Periodic Interrupt Selection

The periodic interrupt allows the $\overline{\text{IRQ}}$ pin to be triggered from once every 500ms to once every 30.517μs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Table 4 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit. Similarly the periodic interrupt is enabled the PIE bit in Register B. Periodic interrupt is usable by practically all real-time systems. It can be used to scan for all forms of input from contact closures to serial receive bits. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.

Table 4 **Periodic Interrupt Rate and Square Wave Output Frequency**

Rate Select Control Register 1				4.194304 or 1.048576MHz Time Base		32.768kHz Time Base	
				Periodic Interrupt Rate t_{PI}	SQW Output Frequency	Periodic Interrupt Rate t_{PI}	SQW Output Frequency
RS3	RS2	RS1	RS0				
0	0	0	0	None	None	None	None
0	0	0	1	30.517μs	32.768kHz	3.90625ms	256Hz
0	0	1	0	61.035μs	16.384kHz	7.8125ms	128Hz
0	0	1	1	122.070	8.192kHz	122.070μs	8.192kHz
0	1	0	0	244.141μs	4.096kHz	244.141μs	4.096kHz
0	1	0	1	488.281μs	2.048kHz	488.281μs	2.048kHz
0	1	1	0	976.562μs	1.024kHz	976.562μs	1.024kHz
0	1	1	1	1.953125ms	512Hz	1.953125ms	512Hz
1	0	0	0	3.90625ms	256Hz	3.90625ms	256Hz
1	0	0	1	7.8125ms	128Hz	7.8125ms	128Hz
1	0	1	0	15.625ms	64Hz	15.625ms	64Hz
1	0	1	1	31.25ms	32Hz	31.25ms	32Hz
1	1	0	0	62.5ms	16Hz	62.5ms	16Hz
1	1	0	1	62.5ms	8Hz	125ms	8Hz
1	1	1	0	250ms	4Hz	250ms	4Hz
1	1	1	1	500ms	2Hz	500ms	2Hz

Update Cycle

The 146818 executes an update cycle once-per-second, assuming one of the proper time bases is in place, the divider is not clear, and the SET bit in register B is clear. The SET bit in the "1" state permits the program to initialise the time and calender bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 4.194304MHz or 1.048576MHz time base the update cycle takes 248 μs while a 32.768kHz time base update cycle takes 1984 μs. During the update cycle, the time, calendar, and alarm bytes are not accessible by the processor program. The 146818 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update in progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating non-availability during update are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a sub-routine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999ms are available to read valid time and data information. During this time a display could be updated or the information could be transferred to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second.

Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes "1", the update cycle begins 244 μs later. Therefore, if a "0" is read on the UIP bit, the user has at least 244 μs before the time/calendar data will be changed. If a "1" is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 μs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set "1" between the setting of the PF bit in Register C (Figure 14) Periodic interrupts that occur at a rate of greater than $t_{BUC} + t_{UC}$ allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within ($t_{PI} \div 2$) + t_{BUC} to insure that data is not read during the update cycle.

Power-down Considerations

In most systems, the 146818 must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made. During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimise power consumption, and ensure hardware reliability.

The chip enable ($\overline{CE}$) pin controls all bus inputs ($\overline{R/W}$, DS, AS, $AD_0 - AD_7$). $\overline{CE}$, when negated, disallows any unintended modification of the RTC data by the bus. CE also reduces power consumption by reducing the number of transitions seen internally.
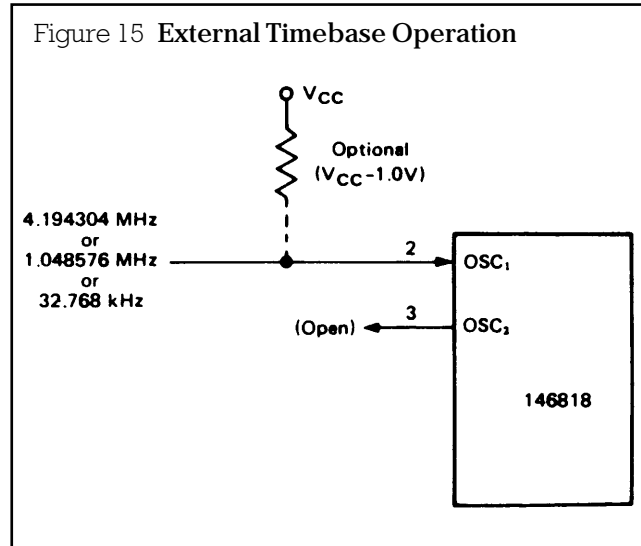
Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the square-wave (SQW) pin.

During and after the power source conversion, the V_{IN} maximum specification must never be exceeded. Failure to meet the V_{IN} maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part.

Figure 14 **Update-Ended and Periodic Interrupt Relationship**

SIGNAL DESCRIPTIONS

The block diagram in Figure 9, shows the pin connection with the major internal functions of the 146818 Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

V_{CC}, V_{SS}

DC power is provided to the part on these two pins, V_{CC} being the most positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

OSC_1, OSC_2 - Time Base (Inputs)

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304MHz, 1.048576MHz, or 32.768kHz may be connected to OSC_1 as shown in Figure 15. The time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant crystal at 4.194304MHz, 1.048576MHz or 32.768kHz frequencies. The crystal connections are shown in Figure 10.

Figure 15 **External Timebase Operation**
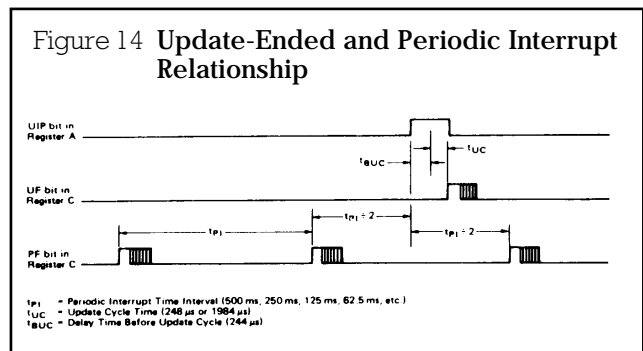
CKOUT - Clock Out (Output)

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 5.

CKFS - Clock Out Frequency Select (Input)

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. CKFS tied to V_{CC} causes CKOUT to be the same frequency as the time base at the OSC_1 pin. When CKFS is at V_{SS}, CKOUT is the OSC_1 time-base frequency divided by four. Table 5 summarises the effect of CKFS.

Table 5 **Clock Output Frequencies**

Time Base (OSC_1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4.194304MHZ	"High"	4.194304MHz
4.194304MHz	"Low"	1.048576MHz
1.048576MHz	"High"	1.048576MHz
1.048576MHz	"Low"	262.144kHz
32.768kHz	"High"	32.768kHz
32.768kHz	"Low"	8.192kHz

SQW - Square-Wave (Output)

The SQW pin can output a signal from one of 15 of the 22 internal-divider stages. The frequency and output enable of the SQW may be altered by programming Register A, as shown in Table 4. The SQW signal may be turned on and off using a bit in Register B.

AD$_0$–AD$_7$ - Multiplexed Bidirectional Address/ Data Bus

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the 146818 since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the 146818 latches the address from AD$_0$ to AD$_5$. Valid write data must be presented and held stable during the latter portion of the DS or $\overline{\text{WR}}$ pulses. In a read cycle, the 146818 outputs 8 bits of data during the latter portion of the DS or $\overline{\text{RD}}$ pulses, then ceases driving the bus (returns the output drivers to three-state) when DS falls in the 6800 case or $\overline{\text{RD}}$ rises in the other case.

AS - Multiplexed Address Strobe (Input)

A positive going multiplexed address strobe pulse serves to de-multiplex the bus. The falling edge of AS or ALE causes the address to be latched within the 146818. The bus control circuit in the 146818 also latches the state of the DA pin with the falling edge of AS or ALE.

DS - Data Strobe or Read (Input)

The DS pin has two interpretations via the bus control circuit. When emanating from 6800 family type processor, DS is a positive pulse during the latter portion of the bus cycle, and is called DS (data strobe), E (enable), and Ø2 (Ø2 clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.

The second interpretation of DS is that of $\overline{\text{RD}}$, $\overline{\text{MEMR}}$, or $\overline{\text{I/OR}}$ emanating from the 8085 type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. The interpretation of DS is also the same as an output-enable signal on a typical memory.

The bus control circuit, within the 146818, latches the state of the DS pin on the falling edge of AS/ALE. In 6800 mode, DS must be "Low" during AS/ALE, which is the case with 6800 family multiplexed bus processors. To insure the 8085 mode of this circuit the DS pin must remain "High" during the time AS/ALE is "High".

R/$\overline{\text{W}}$ - Read/Write (Input)

The bus control circuit treats the R/$\overline{\text{W}}$ pin in one of two ways. When a 6800 family type processor is connected, R/$\overline{\text{W}}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with "High" level on R/$\overline{\text{W}}$ while DS is "High", whereas a write cycle is a "Low" on R/$\overline{\text{W}}$ during DS.

The second interpretation of R/$\overline{\text{W}}$ is as a negative write pulse, $\overline{\text{WR}}$, $\overline{\text{MEMW}}$, and $\overline{\text{I/OW}}$ from 8085 type processors. This circuit in this mode gives R/$\overline{\text{W}}$ pin the same meaning as the write ($\overline{\text{W}}$) pulse on many generic RAMs.

$\overline{\text{CE}}$ - Chip Enable (Input)

The chip-enable ($\overline{\text{CE}}$) signal must be asserted ("Low") for a bus cycle in which the 146818 is to be accessed. $\overline{\text{CE}}$ is not latched and must be stable during DS and AS (in the 6800 case) and during $\overline{\text{RD}}$ and $\overline{\text{WR}}$ (in the 8085 Case). Bus cycles which take place without asserting $\overline{\text{CE}}$ cause no actions to take place within the 146818. When $\overline{\text{CE}}$ is "High", the multiplexed bus output is in a high-impedance state.

When $\overline{\text{CE}}$ is "High", all address, data, DS, and $\overline{\text{R/W}}$ inputs from the processor are disconnected within the 146818.

This permits the 146818 to be isolated from a powered-down processor. When $\overline{\text{CE}}$ is held "High", an unpowered device cannot receive power through the input pins from the real-time clock power source. Battery power consumption can thus be reduced by using a pull-up resistor or active clamp on $\overline{\text{CE}}$ when the main power is off.

$\overline{\text{IRQ}}$ - Interrupt Request (Output)

The $\overline{\text{IRQ}}$ pin is an active "Low" output of the 146818 that may be used as an interrupt input to a processor. The $\overline{\text{IRQ}}$ output remains "Low" as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. To clear the $\overline{\text{IRQ}}$ pin, the processor program normally reads Register C. The $\overline{\text{RES}}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{\text{IRQ}}$ level is in the high-impedance state. Multiple interruption devices may thus be connected to an $\overline{\text{IRQ}}$ bus with one pull-up at the processor.

$\overline{\text{RES}}$ - Reset (Input)

The $\overline{\text{RES}}$ pin does not affect the clock, calendar, or RAM functions. On powerup, the $\overline{\text{RES}}$ pin must be held "Low" for the specified time, t$_{\text{RLH}}$, in order to allow the power supply to stabilise. Figure 16 shows a typical representation of the $\overline{\text{RES}}$ pin circuit.
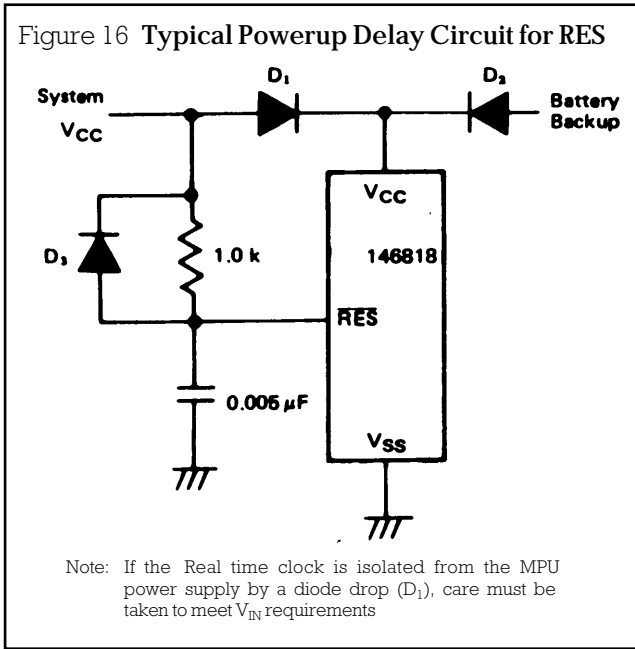
When $\overline{\text{RES}}$ is "Low" the following occurs:

a) Periodic Interrupt Enable (PIE) bit is cleared to "0".

b) Alarm Interrupt Enable (AIE) bit is cleared to "0".

c) Update ended interrupt Enable (UIE) bit is cleared to "0".

d) Update ended Interrupt Flag (UF) bit is cleared to "0".

e) Interrupt Request status Flag (IRQF) bit is cleared to "0".

f) Periodic Interrupt Flag (PF) bit is cleared to "0".

g) Alarm Interrupt Flag (AF) bit is cleared to "0".

h) $\overline{\text{IRQ}}$ pin is in high-impedance state, and

i) Square-Wave output Enable (SQWE) bit is cleared to "0".

● PS - Power Sense (Input)

The power-sense pin is used in the control of the valid RAM and time (VRT) bit in Register C. When the PS pin is "Low" the VRT bit is cleared to "0".

During powerup, the PS pin must be externally held "Low" for the specified time, t$_{\text{PLH}}$. As power is applied the VRT bit remains "Low" indicating that the contents of the RAM, time registers, and calendar are not guaranteed. When normal operation commences PS should be permitted to go "High". Figure 17 shows a typical circuit connection for the power-sense pin.

Figure 16 **Typical Powerup Delay Circuit for RES**

Note: If the Real time clock is isolated from the MPU power supply by a diode drop (D₁), care must be taken to meet V_{IN} requirements

REGISTERS

The 146818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Register A ($0A)

MSB   LSB

b7	b6	b5	b4	b3	b2	b1	b0	Read/Write
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Register except UIP

UIP - The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 µs (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero - it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibit any update cycle and then clear the UIP status bit.

Table 6 **Update Cycle Times**

UIP Bit	Time Base (OSC₁)	Update Cycle Time (t$_{UC}$)	Minimum Time Before Update Cycle (t$_{BUC}$)
1	4.194304MHz	248µs	-
1	1.048576MHz	248µs	-
1	32.768kHz	1984µs	-
0	4.194304MHz	-	244µs
0	1.048576MHz	-	244µs
0	32.768kHz	-	244µs

DV2, DV1, DV0 - Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 3 shows that time bases of 4.194304MHz, 1.048576MHz, and 32.768kHz may be used. The divider selection bits are also used to reset the divider chain. When the time-calendar is first initialised, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed the first update cycle begins one second later. These three read/write bits are never modified by the RTC and are not affected by $\overline{RES}$.

RS₃, RS₂, RS₁, RS₀ - The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate an output square-wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 4 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the **RS** bits. These four bits are read/write bits which are not affected by $\overline{RES}$ and are never changed by the RTC.

Register B ($0B)

MSB   LSB

b7	b6	b5	b4	b3	b2	b1	b0	Read/Write
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Register

Note: DSE (Daylight Save Enable) is not available on RS146818 ic's.

SET - When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialise the time and calendar bytes without an update occurring in the midst of initialising. SET is a read/write bit which is not modified by RES or internal functions of the 146818.

PIE - The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit to cause the $\overline{IRQ}$ pin to be driven "Low". A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Control Register A. A "0" in PIE blocks $\overline{IRQ}$ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still at the periodic rate. PIE is not modified by any internal 146818 functions, but is cleared to "0" by a RES.

AIE - The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an IRQ signal. The RES pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE - The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flag 9UF) bit to assert $\overline{IRQ}$. The $\overline{RES}$ pin going "Low" or the SET bit going "1" clears the UIE bit.
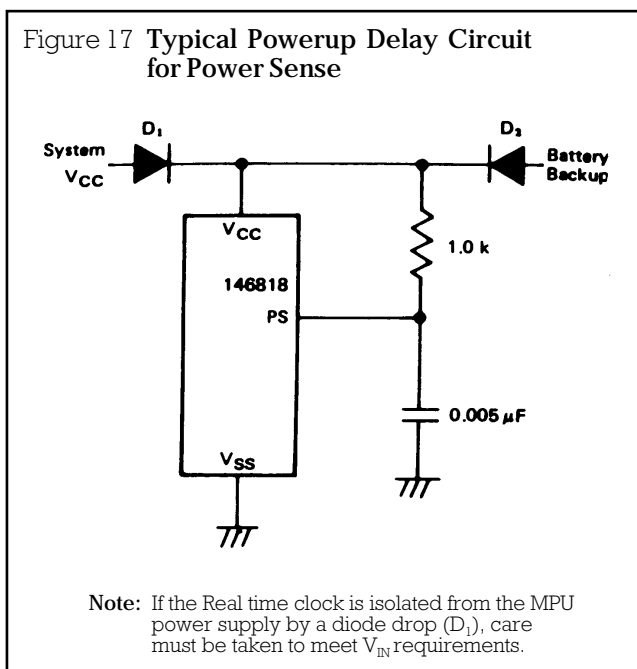
SQWE - When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a "0" the SQW pin is held "Low". The state of SQWE is cleared by the $\overline{RES}$ pin. SQWE is a read/write bit.

DM - The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or RES. A "1" in DM signifies binary data, while a "0" in DM specified binary-coded-decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by the software.

Register C ($0C)

MSB   LSB

b7	b6	b5	b4	b3	b2	b1	b0	Read-Only
IRQF	PF	AF	UF	0	0	0	0	Register

Figure 17 **Typical Powerup Delay Circuit for Power Sense**

Note: If the Real time clock is isolated from the MPU power supply by a diode drop (D_1), care must be taken to meet V_{IN} requirements.

IRQF - The interrupt request flag (IRQF) is set to a "1" when one or more of the following is true:

PF = PIE = "1"

AF = AIE = "1"

UF = UIE = "1"

i.e., IRQF = PF.PIE + AF.AIE + UF.UIE

Any time the IRQF bit is a "1", the $\overline{IRQ}$ pin is driven "Low". All flag bits are cleared after Register C is read by the program or when the $\overline{RES}$ pin is low. A program write to Register C does not modify any of the flag bits.

PF - The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an IRQ signal and the IRQF bit when PIE is also a "1". The PF bit is cleared by a RES or a software read of Register C.

AF - A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the $\overline{IRQ}$ pin to go "Low", and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A RES or a read of Register C clears AF.

UF - The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting $\overline{IRQ}$. UF is cleared by a Register C read or a $\overline{RES}$.

b3 to b0 - The unused bits of Status Register C are read as "0s". They can not be written.

Register D ($0D)

MSB   LSB

b7	b6	b5	b4	b3	b2	b1	b0	Read Only
VRT	0	0	0	0	0	0	0	Register

VRT - The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is "Low". The processor program can set the VRT bit when the time and calendar are initialised to indicate that the RAM and time are valid. The VRT is a read/only bit which is not modified by the $\overline{RES}$ pin. The VRT bit can only be set by reading the Register D.

b6 to b0 - The remaining bits of Register D are unused. They cannot be written, but are always read as "0s".

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