Densitron

Novel Engineering Worldwide Solutions

HD61830 / HD61830B LCD Graphics Controller Chip.

Application Notes

---

1. INTRODUCTION

The HD61830(B) graphics controller chip is designed to control small to medium size graphic Liquid Crystal Display modules (LCD). It may be interfaced with a number of different 8-bit micro-processor units (MPU). It provides the necessary interface between the MPU and the video RAM (VRAM), sometimes referred to as Display RAM or Refresh RAM. It also generates the necessary timing and data signals for the liquid crystal driver circuits. It has a built-in 192 character Character-Generator ROM (CG-ROM) and Character Generator (CG) circuits. The HD61830(B) has the capability to control upto 64K bytes of external display RAM in graphics mode and 4K bytes in the character mode. Most designs using the HD61830(B) only implement 2K to 8K of VRAM depending on the size of LCD screen. This VRAM may be allocated for text or graphics. The HD61830(B) can support a wide variety of LCD formats.

This application note is not written with any specific display in mind but is intended to give a thorough understanding of how to use the HD61830(B) and implement the software/hardware interface. Some LCD modules will have the HD61830(B) controller built into the module such as the LM31XX and LM41XX series of LCD modules, others require an external graphics controller. This application note is applicable to the LM1001GC, LM1002GC and LM1006GC graphics controller cards available from Densitron as well as to Densitron LCD modules with on-board HD61830(B) graphics controllers.

---

2. Main Functions and Features of the HD61830

- Simple 8-bit parallel Interface
- Built in Character Generator and font table (160, 5x7 plus 32, 5x11 characters)
- External CG-ROM option for upto 256 character font table
- Software Selectable Cursor ON/OFF/BLINK attributes
- Software instructions for scrolling, character blink and bit manipulation
- Software Selectable Character or Graphics modes
- Software selectable Duty (1 to 1/128)
- Software Selectable Character Cell size (6x8 upto 8x16)
- Low power CMOS design

Note: Not all these features are implemented on Densitron LCD modules or LM100X series controller cards.

---

3. Electrical Specifications for HD61830/HD61830B

3.1 Absolute Maximum Ratings

Item	Symbol	Value	Units
Power supply voltage	V_{CC}	-0.3 to 7.0	V
Input voltage	V_{in}	-0.3 to V_{CC}+0.3	V
Operating Temperature	T_{op}	-20 to 75	°C
Storage Temperature	T_{stg}	-55 to 125	°C

Note:

1. All voltages are referenced to GND=0V
2. Specification is for HD61830(B) only. LCD module specifications may differ.

3.2 Electrical Characteristics

(V_{CC}=+5V±10%, GND=0V, Ta=-20 to +75°C)

Item		Symbol	Condition	Min	Max	Units	Notes
Input voltage	"H"	V_{IH}		2.2	V_{CC}	V	1, 4
(TTL Level)	"L"	V_{IL}		0	0.8	V	1, 2, 4
	"H"	V_{IHR}		3.0	V_{CC}	V	2
Input voltage	"H"	V_{IHC}		$0.7V_{CC}$	V_{CC}	V	3, 7
(CMOS Level)	"L"	V_{ILC}		0	$0.3V_{CC}$	V	3, 7
Output voltage	"H"	V_{OH}	$-I_{OH}$=0.6mA	2.4	V_{CC}	V	4
(TTL level)	"L"	V_{OL}	I_{OL}=1.6mA	0	0.4	V	4
Output voltage	"H"	V_{OHC}	$-I_{OH}$=0.6mA	V_{CC}-0.4	V_{CC}	V	5, 6
(CMOS level)	"L"	V_{OLC}	I_{OL}=0.6mA	0	0.4	V	5, 6
Input leakage current		I_{IL}	V_{in}=0~V_{CC}	-5	5	µA	4
Output leakage current		I_{OL}	V_{out}=0~V_{CC}	-10	10	µA	4
Internal Oscillation		f_{osc}	C_f=15p±5% R_f=39K±2% f_{osc}=500KHz	400	600	KHz	3
External clock frequency		f_{cp}		100 100	1100 2400	KHz	37
External clock Duty		Duty		47.5	52.5	%	3, 7
Ext. clock rise/fall time		t_{rcp}, t_{fcp}		-	50 25	ns	3 7

Notes:

1. E, (Not CS), RS, R/(Not W)
2. (Not RST)
3. CR for HD61830
4. DB0 to DB7
5. FLM, CL1, CL2
6. D1, D2, M
7. CR for HD61830B

---

4. Interface Pin Connections

4.1 MPU Interface Pin Functions

Pin-outs differ for individual LCD modules with on-board controllers. Please refer to individual module data sheets for pin assignment information.

Pin Name	I/O	Pin Function
V_{SS}	-	Ground
V_{CC}	-	Logic Supply (+5V)
RS	I	Register Select: "1" = Instruction Register "0" = Data Register
R/(Not W)	I	Read/Write: "1" = Read from HD61830(B) "0" = Write to HD61830(B)
E	I	Enable (Active High)
DB0	I/O	Bi-directional Data Bus Line 0
DB1	I/O	Bi-directional Data Bus Line 1

DB1	I/O	Bi-directional Data Bus Line 1
DB2	I/O	Bi-directional Data Bus Line 2
DB3	I/O	Bi-directional Data Bus Line 3
DB4	I/O	Bi-directional Data Bus Line 4
DB5	I/O	Bi-directional Data Bus Line 5
DB6	I/O	Bi-directional Data Bus Line 6
DB7	I/O	Bi-directional Data Bus Line 7
(Not CS)	I	Chip Select (Active Low)
(Not RST)	I	Reset (Active Low)

4.2 LCD Interface Pin Functions

For LCD modules with on-board controllers, these signals are not generally accessible. However for the LM1001GC, LM1002GC and LM1006GC graphics controller cards these signals are available; refer to individual data sheets for pin assignments.

Pin Name	I/O	Pin Function
D1	O	Serial Data Line 1
FLM	O	First Line Marker (Start of Frame)
M	O	Control Signal for AC drive of LC
CL1	O	Latch clock
CL2	O	Shift clock for serial data
D2	O	Serial Data Line 2
V_{DD}	-	Power supply for logic circuits
V_{SS}	-	Ground
V_{EE}	-	Power supply for LC drivers
V_O	-	Operating voltage for LC drivers (Contrast)

---

5. Timing Characteristics

5.1 MPU Interface Timing (MPU - HD61830)

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time		t_{CYC}	1.0	-	-	µs
Enable pulse width	"H"	t_{WEH}	0.45	-	-	µs
	"L"	t_{WEL}	0.45	-	-	µs
Enable rise time		t_{Er}	-	-	25	ns
Enable fall time		t_{Ef}	-	-	25	ns
Set up time		t_{AS}	140	-	-	ns
Data set up time		t_{DSW}	225	-	-	ns
Data delay time		t_{DDR}	-	-	225	ns
Data hold time (Write)		t_{DHW}	10	-	-	ns
Address hold time		t_{AH}	10	-	-	ns
Data Hold Time (Read)		tDH	20	-	-	ns
Pulse width of /RES		t_{WRES}	1µs	-	2ms	-

Note: MPU interface timing for HD61830B is identical to HD61830

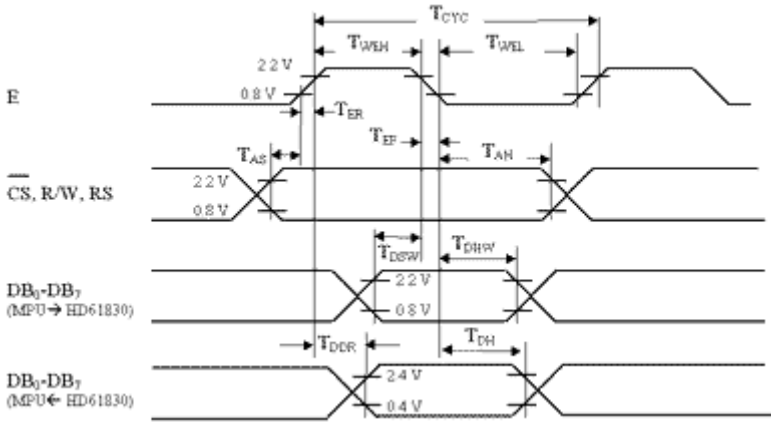


Figure 5.1: MPU Interface Timing (MPU - HD61830(B))

5.2 LCD Interface Timing (HD61830 - LCD)

Item		Symbol	Min	Typ	Max	Unit
Clock pulse width (high level)		t_{WCL1}	450	-	-	ns
Clock delay time		t_{DCL2}	-	-	200	ns
Clock cycle time		t_{WCL2}	900	-	-	ns
Clock pulse width	"H"	t_{WCH}	450	-	-	ns
	"L"	t_{WCL}	450	-	-	ns
M delay time		t_{MD}	-	-	300	ns
FLM delay time		t_{DF}	-	-	300	ns
Data delay time		t_{DD}	-	-	200	ns
Data set up time		t_{SD}	250	-	-	ns

Note: No load is applied to all outputs.

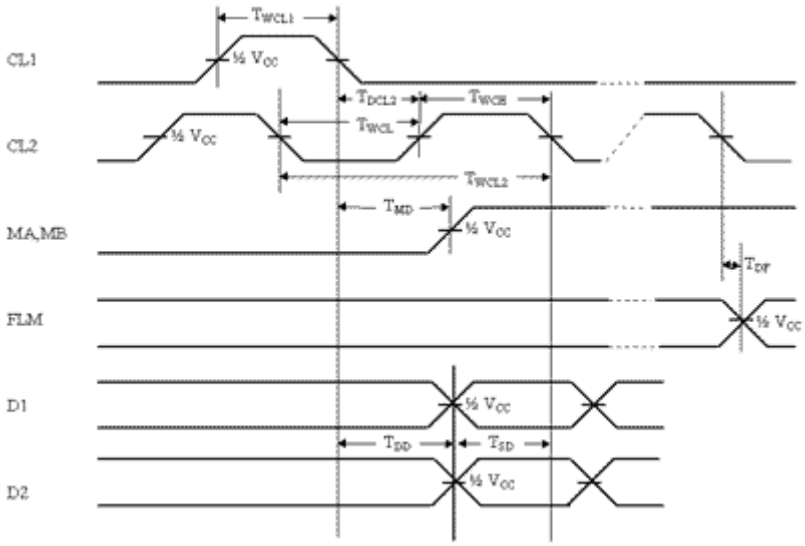
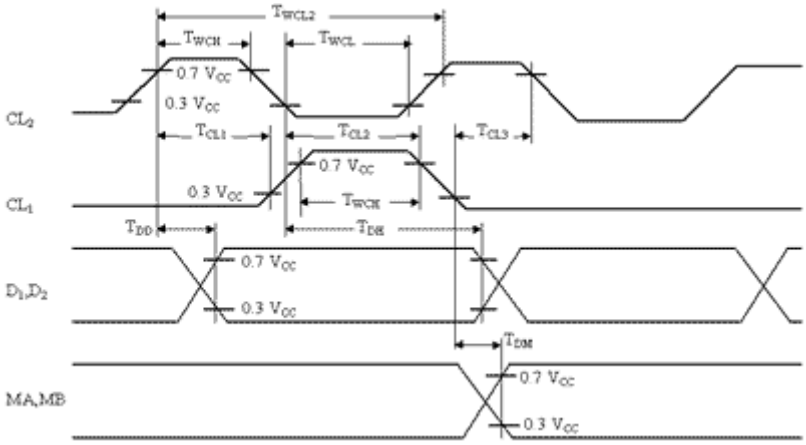


Figure 5.2: LCD Interface Timing (HD61830 - LCD)

5.3 LCD Interface Timing (HD61830B - LCD)

Item		Symbol	Min	Typ	Max	Unit	Note
Clock cycle time		t_{WCL2}	416	-	-	ns	1
Clock pulse width	"H"	t_{WCH}	150	-	-	ns	1
	"L"	t_{WCL}	150	-	-	ns	1
Data delay time		t_{DD}	-	-	50	ns	1
Data hold time		t_{DH}	100	-	-	ns	1
M delay time		t_{DM}	-200	-	200	ns	1
FLM set up time		t_{SF}	400	-	-	ns	2
FLM hold time		t_{HF}	1000	-	-	ns	2
M set up time		t_{SMA}	400	-	-	ns	2
M hold time		t_{HMA}	1000	-	-	ns	2

Note 1 -



Note 2 -

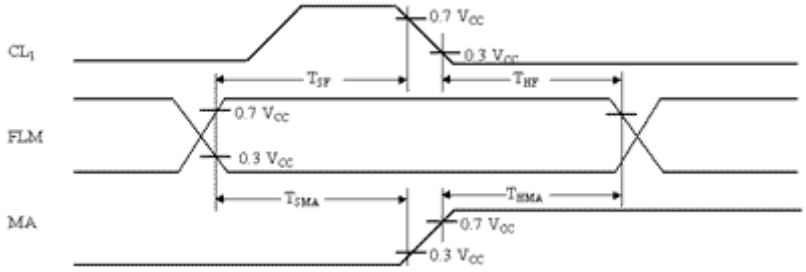


Figure 5.3: LCD Interface Timing (HD61830B - LCD)

---

6. System Block Diagram

All liquid crystal displays require two power sources V_{CC} for logic circuits and V_{EE} for Liquid Crystal (LC) drive. Some graphics LCD modules will run directly of a single V_{CC} supply by generating the V_{EE} voltage on-board; others will require an external DC-DC converter to generate the negative V_{EE} voltage. Refer to individual specifications for details.

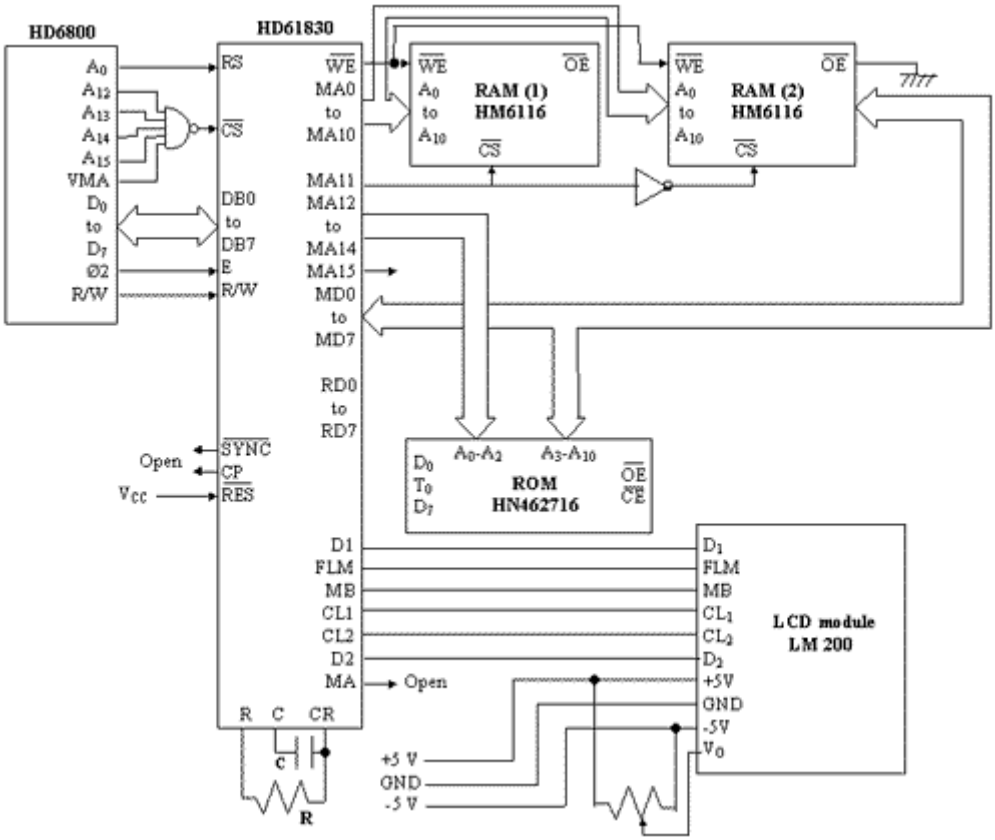


Figure 6.1: System Block Diagram

7. Power Supply Sequencing and (Not RST) Terminal

To prevent latch-up of the CMOS LSI (HD61830(B) and LCD driver LSI) ensure your systems power supply follows the following sequence. The V_{DD} must be applied with a small time delay befor V_{EE} is turned on. It is very important to follow this sequence in order to prevent the CMOS LSI from latching up and to prevent DC signals from being applied to the LC material. If the V_{EE} voltage is applied before the timing signals M, CL1, CL2, and FLM then a DC voltage will be applied to the LC material. Over time this will degrade the LC fluid performance due to their electro-chemical behavior. If this power-up sequence is not adhered to, permanent damage to the LCD module may result.

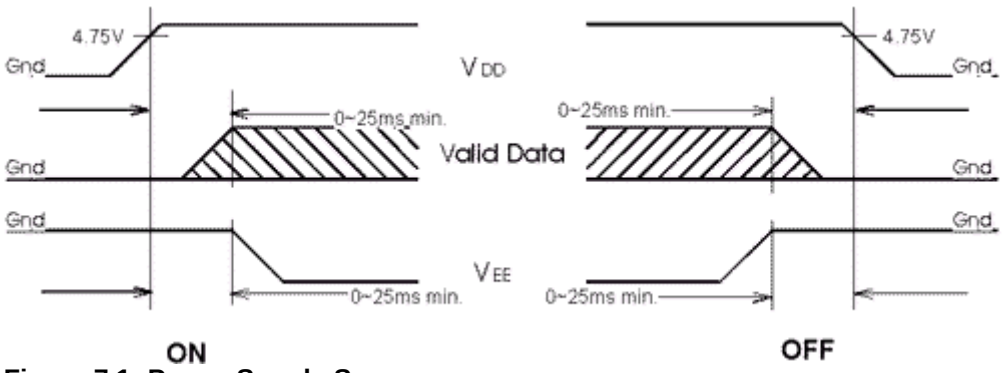


Figure 7.1: Power Supply Sequence

The RESET circuit shown in Figure 7.2 is recommended to correctly reset the HD61830(B). On RESET the internal registers of the HD61830(B) are cleared and the BUSY flag is reset, Display is turned off, H_P=6 and HD61830 is set for Slave mode (Refer to section 8 for detail).

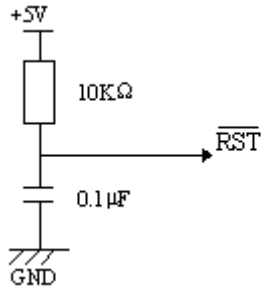


Figure 7.2: RESET Circuit

---

8. HD61830(B) Instruction Set

The following is a summary of available instructions for use with the HD61830(B).

Table 8.0: HD61830(B) Instruction Set

R/Not W	RS	DB7 MSB	DB6	DB5	DB4	DB3	DB2	DB1	DB0 LSB	Function
0	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Set Mode Control Register**
0	0	0	0	Mode Control data						Mode Control data
0	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**Set Character Pitch Register**
0	0	(V_P-1) binary				0	(H_P-1) binary			Vert./Horiz. Pitch data
0	1	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**Set Horizontal Count Register**
0	0	0	(H_N-1) binary							Horizontal Count data
0	1	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Set Multiplex Ratio Register**
0	0	0	(N_X-1) binary							Multiplex ratio data (1/Duty-1)
	1	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**Set Cursor Position Register**
0	0	0	0	0	0	(C_P-1) binary				Cursor Position data
0	1	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**Set Lower Dis. Start Addr Reg**
0	0	(Low order Display Start Address) binary								Lower Display Start Addr. data
0	1	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**Set Upper Dis. Start Addr Reg**
0	0	(High order Display Start Address) binary								Upper Display Start Addr. data
0	1	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**Set Lower Cursor Addr Reg**
0	0	(Low order Cursor Address) binary								Lower Cursor Address data
0	1	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**Set Upper Cursor Addr Reg**
0	0	(High order Cursor Address) binary								Upper Cursor Address data
0	1	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**Write-VRAM Instruction**
0	0	MSB (Character code or bit-map data) LSB								Display data
0	1	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**	**Read-VRAM Instruction**
1	0	MSB (Character code or bit-map data) LSB								Display data
0	1	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**Bit Clear Instruction**
0	0	0	0	0	0	0	(N_B-1) binary			Bit Address
0	1	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**Bit Set Instruction**
0	0	0	0	0	0	0	(N_B-1) binary			Bit Address
1	1	**BF**	*	*	*	*	*	*	*	**Read BUSY FLAG**

Note:

1. * = DON'T CARE
2. Read the status of the Busy Flag before each new instruction is sent to the HD61830(B). If the

HD61830(B) Busy Flag is set (BF=1) then the HD61830(B) is busy processing the previous instruction. If a new instruction is sent to the HD61830(B) while the Busy Flag, BF=1, then that command shall be ignored by the HD61830(B).

3. Vertical Character Pitch, V_P:$0 \leq (V_P-1) \leq 15$
4. Horizontal Character Pitch,H_P:$5 \leq (H_P-1) \leq 7$
5. Horizontal Character Count, H_N:$H_N \leq 128$, H_N must be an even integer.
6. Multiplex Ratio, N_X: N_X=1/Duty, $N_X \leq 128$

8.1 Mode Control Register

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Set Mode Control Register**
0	0	0	0	D5	D4	D3	D2	D1	D0	Mode Control data
				|	|	|	|	|	**0**	HD61830(B) Internal CG ROM
				|	|	|	|	**1**	External CG ROM
				|	|	|	**0**	--	Character mode
				|	|	|	**1**	--	Graphics mode
				|	|	**0**	**0**	--	--	Cursor OFF
				|	|	**0**	**1**	--	--	Cursor ON
				|	|	**1**	**0**	--	--	Cursor OFF Character Blink
				|	|	**1**	**1**	--	--	Cursor blank
				|	**0**	--	--	--	--	Slave Mode
				|	**1**	--	--	--	--	Master Mode
				0	--	--	--	--	--	Display OFF
				1	--	--	--	--	--	Display ON

The Mode Control register sets the operating mode for the HD61830(B). It controls the character/graphics mode, cursor, on/off/blink, master/slave and display on/off. When D1 is set to 1 and D0, D2 and D3 are set to 0, the HD61830(B) is set to graphics mode and the character generator and cursor functions are disabled.

Most displays and controller cards use only one HD61830 so D4=1. The LM1006GC is the exception as two HD61830 are used; one configured as the slave (D4=0) and the other as the master (D4=1).

8.2 Character Pitch Register

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Set Character Pitch Register**
0	0	(V_P-1) binary				0	(H_P-1) binary			Vert./Horiz. Pitch data

Character Mode: V_P and H_P set the horizontal and vertical size of each character cell. To display the 5x11 font stored in the CG-ROM set V_P=12 and H_P=6. That is set the Character Pitch register to B5H. If displaying only the 5x7 font then set VP=8 and HP=6. That is set the Character Pitch register to 75H. A value in the range of 1 to 16 may be used for V_P. A value in the range of 6 to 8 may be used for H_P. Refer to section 9.0 for pictorial definitions of V_P and H_P.

Graphics Mode: V_P has no meaning in Graphics mode and may be set to any value. H_P should be set to 8. That is set Character Pitch register to 07H for Graphics mode.

8.3 Horizontal Count Register

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	1	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**Set Horizontal Count Instruction**
0	0	0	(H_N-1) binary							Horizontal Count data

Character Mode: This register sets the number of horizontal characters that can be displayed on the LCD. The character width is defined by H_P in the Character Pitch Register (Section 8.2).

Graphics Mode: This register sets the number of horizontal bytes that can be displayed on the LCD. For graphics mode, it is best to set H_P=8.

If the total number of horizontal dots on the LCD screen is **n** then:

$H_N = n / H_P$

Note: HN must be an even integer value.in the range $2 \leq HN \leq 128$

For example: If using HD61830(B) to control a 64x240 LCD screen in Character Mode, with HP=6 then set HN=28H. That is, write 27H into Horizontal Count register.

8.4 Multiplex Ratio Register (1/Duty)

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	1	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Set Multiplex Ratio Register**
0	0	0	(NX-1) binary							Multiplex ratio data [(1/Duty)-1]

Set N_X to the Duty cycle ratio of the LCD being used. N_X should be in the range $1 \leq N_X \leq 128$.

For example: for a 1/64 duty LCD screen set N_X=64 and write 3FH into Multiplex Ratio register.

8.5 Cursor Position Register

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	1	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**Set Cursor Position Register**
0	0	0	0	0	0	(C_P-1) binary				Cursor Position data

In Character Mode, C_P indicates the position of the cursor within the character cell defined by V_P and H_P in the Character Pitch register (Section 8.2). The horizontal width of the cursor is equal to H_P. A value of 1 to 16 may be set for C_P. If $C_P > V_P$ no cursor will be displayed. If $C_P \leq V_P$ the cursor has higher priority and the cursor shall be written over the top of the character on the LCD screen. C_P=1 means cursor will appear on top row of character cell; if $C_P=V_P$ then cursor will appear on bottom row of character cell.

For example: To display a cursor underneath a 5x7 character, set C_P=8. That is write 07H into Cursor Position register. To display a cursor underneath a 5x11 character, set C_P=12. That is write 0BH into Cursor Position register.

8.6 Display Start Address Registers

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	1	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**Set Lower Dis. Start Addr Reg**
0	0	(Low order Display Start Address) binary								Lower Display start Addr. data
0	1	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**Set Upper Dis. Start Addr Reg**
0	0	(High order Display Start Address) binary								Upper Display Start Addr. data

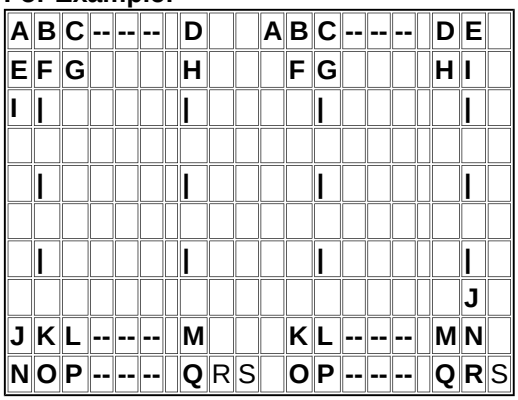
The High and Low order Display Start Address indicates a VRAM address at which the data displayed at the top left corner of the LCD screen is stored.

Character Mode: Set DB7~DB4 = 0, for High order Display Start Address. Only DB3~DB0 is valid for High order Display Start Address in the Character Mode. That is a value in the range of 0000H to 0FFFH may be written into the High/Low order Display Start Address registers for the HD61830(B) Character Mode.

Graphics Mode: All 16 bits of the High/Low order Display Start Address register are valid for the Graphics Mode of the HD61830(B). A value in the range 0000H to FFFFH may be written into the High/Low order Display Start Address registers. However bear in mind that not all LCD modules or controller cards have this much addressable RAM on-board. Refer to individual LCD module specifications for size of addressable VRAM.

The Display Start Address registers are very useful when implementing scrolling both horizontally and vertically. The Display Start Address may be incremented or decremented by the value H_N (section 8.3) to scroll up or down by one row of dots in the Graphics mode or by one character row (set by VP) in the Character mode. By incrementing/decrementing the Display Start Address by one will cause the LCD screen to shift horizontally left/right by the number of dots set by the value H_P (section 8.2) as shown by below.

For Example:



Before Incrementing Display Start Address.... After Incrementing Display Start Address....

8.7 Cursor Address Register (VRAM write address register)

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	1	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**Set Lower Cursor Addr Reg**
0	0	(Low order Cursor Address) binary								Lower Cursor Address data
0	1	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**Set Upper Cursor Addr Reg**
0	0	(High order Cursor Address) binary								Upper Cursor Address data

The Cursor Address registers set the address for reading/writing display data to the VRAM. Always write to the Low Order Cursor Address register first followed by the High order Cursor Address register. The High order Cursor Address register may be updated independently from the Low order Cursor Address register; however if the Low order Cursor Address register is updated then the High order Cursor Address register must also be updated directly afterwards.

The Cursor Address is automatically incremented by +1 after each successive **Write-VRAM, Read-VRAM**, **Bit Set** or **Bit Clear** instruction.

Character Mode: Set DB7~DB4 = 0, for High order Cursor Address. Only DB3~DB0 is valid for High order Cursor Address in the Character Mode. That is a value in the range of 0000H to 0FFFH may be written into the High/Low order Display Start Address registers for the HD61830(B) Character Mode.

Graphics Mode: All 16 bits of the High/Low order Cursor Address register are valid for the Graphics Mode of the HD61830(B). A value in the range 0000H to FFFFH may be written into the High/Low order Cursor Address registers. However bear in mind that not all LCD modules have this much addressable RAM on-board. Refer to individual LCD module specifications for size of addressable VRAM.

8.8 Write Data to VRAM Instruction

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	1	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**Write-VRAM Instruction**
0	0	MSB (Character code or bit-map data) LSB								Display data

Character Mode: This instruction will load the character code data into VRAM at the address specified by the current value stored in the Cursor Address register (section 8.7). The Cursor Address register will increment by +1 after each successive Write-VRAM instruction. Therefore to write ***DENSITRON*** to VRAM address 01FFH, write the following sequence of commands to the HD61830(B):

STEP #	1	2	3	4	5	6	7	8	9	10	11	12	13	14
DB7~DB0	**0A**	FF	**0B**	01	**0C**	44	45	4E	53	49	54	52	4F	4E
RS	**1**	0	**1**	0	**1**	0	0	0	0	0	0	0	0	0
R/Not W	**0**	0	**0**	0	**0**	0	0	0	0	0	0	0	0	0

Note: Check Busy Flag (BF) before steps 1, 3, and 5. All values are hexadecimal.

In order to move the word ***DENSITRON*** so that it is visible at the top left hand corner of the LCD screen set the Display Start Address register to 01FFH (section 8.6). Note that if the character code written to VRAM is not recognized by the CG-ROM then a blank character will be displayed on the LCD screen (Refer to section 14.0).

Graphics Mode: This instruction will load a byte of data into VRAM at the address specified by the current value stored in the Cursor Address (section 8.7). The Cursor Address register will increment by +1 after each successive Write-Vram instruction. The least significant bit (LSB) of each byte written to VRAM correspondes to the left most dot on the LCD screen (See section 10.0)

8.9 Read data from VRAM Instruction

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	1	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**	**Read-VRAM Instruction**
1	0	MSB (Character code or bit-map data) LSB								Display data

This instruction outputs the data stored in the VRAM at the address immediately preceding the current Cursor Address. The Cursor Address is incremented by +1 after each successive Read-VRAM instruction. To read the VRAM data at the current Cursor Address it will be necessary to do a dummy Read-VRAM instruction so that the Cursor address is incremented by +1 before issuing the next read instruction which will put valid data on the data bus. For example assume ***DENSITRON*** is stored in VRAM starting at address 01FFH. The following sequence will read the data stored at addresses 01FFH to 0208H. Note the dummy read at step number 6. It is important to remember to make one dummy read when reading data after setting the Cursor Address register.

STEP #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DB7~DB0	**0A**	FF	**0B**	01	**0D**	*	44	45	4E	53	49	54	52	4F	4E
RS	**1**	0	**1**	0	**1**	0	0	0	0	0	0	0	0	0	0
R/Not W	**0**	0	**0**	0	**0**	1	1	1	1	1	1	1	1	1	1

Note: Check Busy Flag (BF) before steps 1, 3, and 5. All values are hexadecimal.

8.10 Bit Clear and Bit Set Instructions

R/Not W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	1	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**O**	**Bit Clear Instruction**
0	0	0	0	0	0	0	(N_B-1) binary			Bit Address
0	1	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**Bit Set Instruction**
0	0	0	0	0	0	0	(N_B-1) binary			Bit Address

The Clear/Set Bit instructions reset/set 1 bit in a byte of VRAM data to 0 or 1, respectively. The position of the bit in a byte is defined by NB. NB=1 refers to the LSB, D0. NB=8 refers to the MSB, D7.

The Cursor Address is automatically incremented by +1 after execution of these instructions. For example; to clear bit D4 of address 01FFH and set bits D1 and D6 of 0200H use the following sequence:

STEP #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
DB7~DB0	**0A**	FF	**0B**	01	**0E**	04	**0F**	01	**0A**	00	**0B**	02	**0F**	06
RS	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0
R/Not W	**0**	0	**0**	0	**0**	0	**0**	0	**0**	0	**0**	0	**0**	0

Note: Check Busy Flag (BF) before steps 1, 3, 5, 7, 9 and 11. All values are hexadecimal.

8.11 Read BUSY FLAG

R/Not W	**RS**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Function**
1	1	**BF**	*	*	*	*	*	*	*	**Read BUSY FLAG**

This instruction is used to check whether the HD61830(B) is in the BUSY state or not. The BUSY FLAG (BF) should be checked before initiating any instruction to the HD61830(B), except when data is written in the register (RS=1).

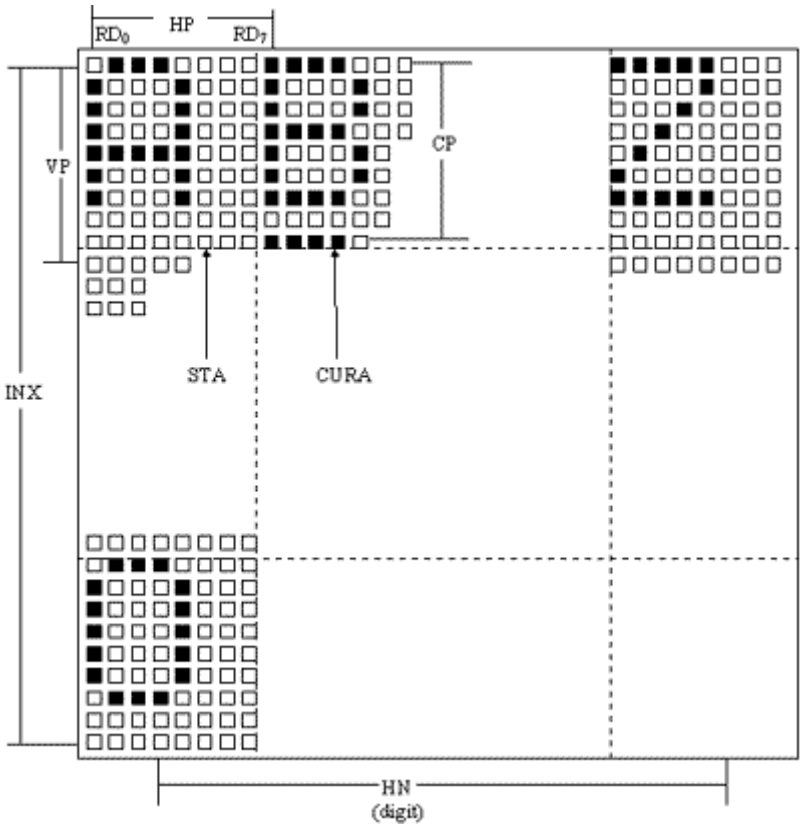
BF=1:HD61830(B) is BUSY
BF=0:HD61830(B) is not BUSY

Table 8.12: Busy Signal Timing

Function	**BUSY**		
	BUSY FLAG	**Min.**	**Max.**
Write Instruction (RS=1)	NOT SET	-	1µs
Write Data (RS=0)	SET	t_{CL2}	2 x t_{CL2}
Read/Write VRAM	SET	2 x t_{CL2}	$(2 + H_P)t_{CL2}$
BIT Set/Clear	SET	$(2 + H_P)t_{CL2}$	$2(H_P+1)t_{CL2}$

Note: A safety factor of 3 times the maximum BUSY time indicated above should be used if the Busy Flag is not polled by the MPU before each instruction is sent to the HD61830(B).

9.0 Definitions for H_P, H_N, V_P, C_P, N_X



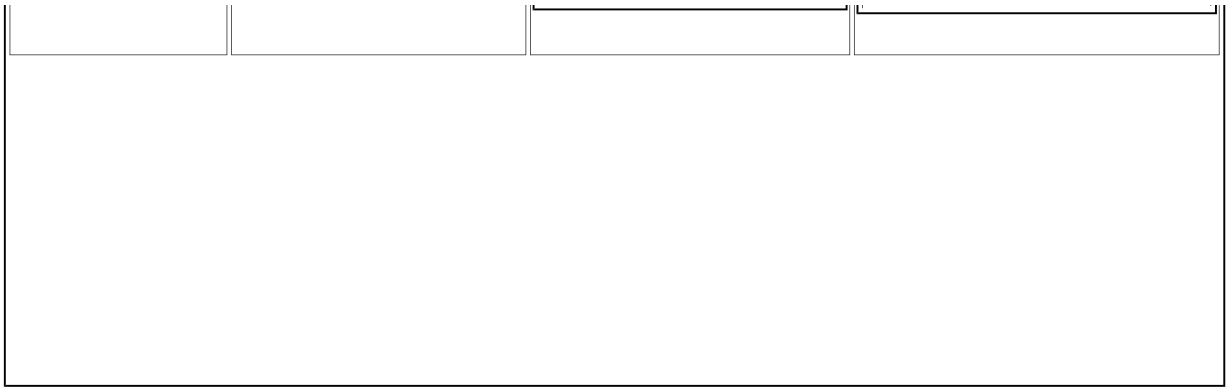
Symbol	Name	Meaning	Value
H_P	Horizontal character pitch	Horizontal character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of horizontal characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode	2 to 128 digits (an even number)
V_P	Vertical character pitch	Vertical character pitch	1 to 16 dots
C_P	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
N_X	Number of time divisions	Inverse of display duty ratio	1 to 128 lines

Note: If the number of vertical dots on the screen is "m", and the number of dots is "n".

$1/m = 1/N_X$ = display duty ratio
$n = H_P \times H_N$, m/V_P = Number of display lines
$C_P \leq V_P$

10.0 Relationship between Display Mode, VRAM data and LCD dots.

Display Mode	Display Data From MPU	RAM	Liquid Crystal Display Panel
Character Display	Character Code (8 bits)	Start address -> b7 b6 b5 b4 b3 b2 b1 b0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 1 0	|<->|H_P A B C



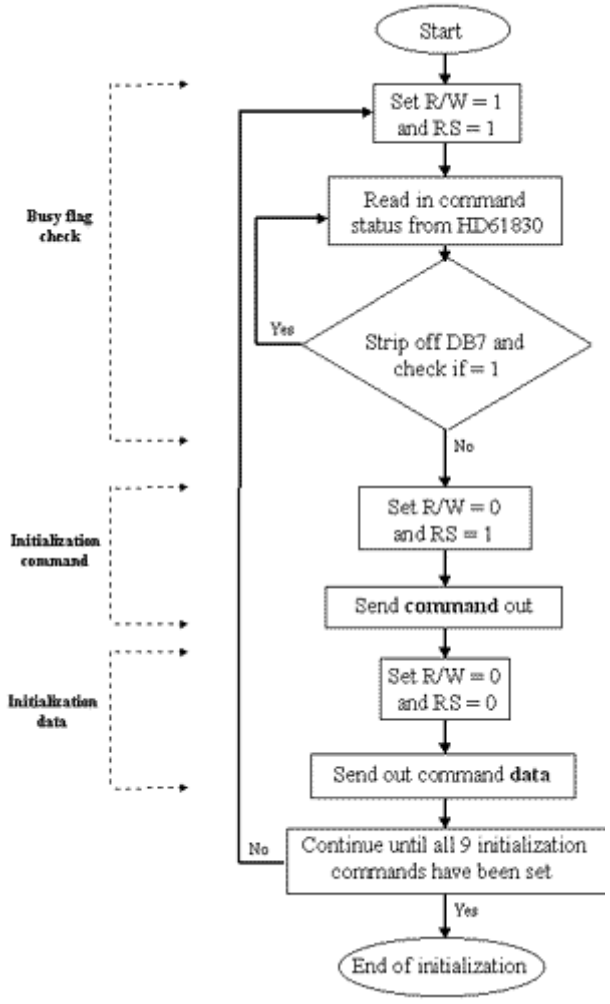
Assume: H_P=6; V_P=8	**LCD Format**		**32 x 128**	**64 x 128**	**64 x 128**	**64 x 240**	**64 x 240**	**64 x 480**	**128 x 128**	**128 x 240**	**128 x 256**
Register/	**LCD Duty**		**1/32**	**1/32**	**1/64**	**1/32**	**1/64**	**1/64**	**1/128**	**1/128**	**1/64**
Data	**R/W**	**RS**									
Mode Control Reg	**0**	**1**	**00H**	**00H**	**00H**	**00H**	**00H**	**00H**	**00H**	**00H**	**00H**
Mode Control data	0	0	34H	34H	34H	34H	34H	34H	34H	34H	34H
Character Pitch Reg	**0**	**1**	**01H**	**01H**	**01H**	**01H**	**01H**	**01H**	**01H**	**01H**	**01H**
Vert/Horiz Pitch data	0	0	75H	75H	75H	75H	75H	75H	75H	75H	75H
Horiz. Count Reg	**0**	**1**	**02H**	**02H**	**02H**	**02H**	**02H**	**02H**	**02H**	**02H**	**02H**
Horiz. Count data (HN-1)	0	0	13H	13H	13H	27H	27H	4FH	13H	27H	29H
Multiplex Ratio Reg.	**0**	**1**	**03H**	**03H**	**03H**	**03H**	**03H**	**03H**	**03H**	**03H**	**03H**
(1/Duty-1), (NX-1)	0	0	1FH	1FH	3FH	1FH	3FH	3FH	7FH	7FH	3FH
Cursor Position Reg	**0**	**1**	**04H**	**04H**	**04H**	**04H**	**04H**	**04H**	**04H**	**04H**	**04H**
Cursor Position	0	0	07H	07H	07H	07H	07H	07H	07H	07H	07H
Start Addr (L) Reg	**0**	**1**	**08H**	**08H**	**08H**	**08H**	**08H**	**08H**	**08H**	**08H**	**08H**
Display Start Addr (L)	0	0	00H	00H	00H	00H	00H	00H	00H	00H	00H
Start Addr (H) Reg	**0**	**1**	**09H**	**09H**	**09H**	**09H**	**09H**	**09H**	**09H**	**09H**	**09H**
Display Start Addr (H)	0	0	00H	00H	00H	00H	00H	00H	00H	00H	00H
Cursor Address (L) Reg	**0**	**1**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**
Cursor Address (L)	0	0	00H	00H	00H	00H	00H	00H	00H	00H	00H
Cursor Address (H) Reg	**0**	**1**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**
Cursor Address (H)	0	0	00H	00H	00H	00H	00H	00H	00H	00H	00H

12.2 Graphics Mode Initialization:

Assume: H_P=8	**LCDFormat**		**32 x 128**	**64 x 128**	**64 x 128**	**64 x 240**	**64 x 240**	**64 x 480**	**128 x 128**	**128 x 240**	**128 x 256**
Register/	**LCD Duty**		**1/32**	**1/32**	**1/64**	**1/32**	**1/64**	**1/64**	**1/128**	**1/128**	**1/64**
Data	**R/W**	**RS**									
Mode Control Reg	**0**	**1**	**00H**	**00H**	**00H**	**00H**	**00H**	**00H**	**00H**	**00H**	**00H**
Mode Control data	0	0	32H	32H	32H	32H	32H	32H	32H	32H	32H
Character Pitch Reg	**0**	**1**	**01H**	**01H**	**01H**	**01H**	**01H**	**01H**	**01H**	**01H**	**01H**
Vert/Horiz Pitch data	0	0	77H	77H	77H	77H	77H	77H	77H	77H	77H
Horiz. Count Reg	**0**	**1**	**02H**	**02H**	**02H**	**02H**	**02H**	**02H**	**02H**	**02H**	**02H**
Horiz. Count data, (HN-1)	0	0	0FH	0FH	0FH	1DH	1DH	3BH	0FH	1DH	1FH
Multiplex Ratio Reg.	**0**	**1**	**03H**	**03H**	**03H**	**03H**	**03H**	**03H**	**03H**	**03H**	**03H**
(1/Duty-1), (NX-1)	0	0	1FH	1FH	3FH	1FH	3FH	3FH	7FH	7FH	3FH
Cursor Position Reg	**0**	**1**	**04H**	**04H**	**04H**	**04H**	**04H**	**04H**	**04H**	**04H**	**04H**
Cursor Position	0	0	07H	07H	07H	07H	07H	07H	07H	07H	07H

Start Addr (L) Reg	**0**	**1**	**08H**	**08H**	**08H**	**08H**	**08H**	**08H**	**08H**	**08H**	**08H**
Display Start Addr (L)	0	0	00H	00H	00H	00H	00H	00H	00H	00H	00H
Start Addr (H) Reg	**0**	**1**	**09H**	**09H**	**09H**	**09H**	**09H**	**09H**	**09H**	**09H**	**09H**
Display Start Addr (H)	0	0	00H	00H	00H	00H	00H	00H	00H	00H	00H
Cursor Address (L) Reg	**0**	**1**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**	**0AH**
Cursor Address (L)	0	0	00H	00H	00H	00H	00H	00H	00H	00H	00H
Cursor Address (H) Reg	**0**	**1**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**	**0BH**
Cursor Address (H)	0	0	00H	00H	00H	00H	00H	00H	00H	00H	00H

12.3 Initialization Flow Diagram



13.0 Trouble shooting Guide

Symptoms	Possible Solutions
Display appears blank	1, 2, 3, 5, 6, 7, 8, 9, 10, 12, 13, 14
Displayed characters entered unreliably or at random	2, 3, 4
Descender characters such as " g, j, y, p, q " etc are broken or do not appear	17, 11
Missing column segments or pixels	13
Excessive heat generated by LSI chips or excessive I_{DD} current	1, 14
Unable to read VRAM or Busy flag	1, 3, 7, 9, 10
EL Backlight will not function or is too dim	15
LED backlight will not function or is too bright or runs too hot	16

Possible Solutions:

1. Check voltage level and polarity of V_{DD} and V_{SS} at display connector. The V_{DD} logic supply voltage should be in the range 4.75VDC < V_{DD} < 5.25VDC with respect to V_{SS}(GND). Also check that V_{DD} and V_{SS} noise, is within limits.
2. Check the pulse width of (Not RST) is within specified limits or the HD61830(B) will not be reset properly and internal registers will not be initialized. Also check when testing numerous displays on the same test set-up that the VDD voltage is turned off before connecting or disconnecting LCD modules. Note that on power-up the contents of the VRAM are not cleared and will contain random data. It is best to set every location of VRAM to a known state as part of any initialization procedure.
3. Check that the positive going enable pulse "E" is at least 450ns wide and that all Hold and Set-up timing requirements are met as shown in section 5.1.
4. Ensure that data is not being transmitted too fast to the HD61830. Always pole the BUSY flag before sending instructions (section 8.11). If MPU is not reading the BUSY flag before writing instructions, allow an adequate delay between instructions. .
5. Check the voltage level at the V_0 pin is at the correct voltage for the ambient temperature conditions as specified by individual LCD module data sheets.
6. Check the continuity of the cable between the host MPU and the LCD module. Check for broken connections, loose crimps or dry joints on soldered connections. Minimize the length of this cable to reduce cross-talk and noise pick-up. (about 50cm)
7. Check that the data bus of the HD61830 (DB0-DB7) is not excessively loaded during read operations.
8. Check the voltage levels of input signals is as specified by the LCD module data sheet.
9. Check that no more than one external bus device is selected during read operations so as to cause bus contention and erroneous data transfer.
10. Check for damage to PCB traces and plated through Via holes.
11. Check that LCD module has been initialized for correct DUTY cycle. and V_P and H_P are correctly set for 5x11 font (section 8.2).
12. Check that Display ON/OFF flag is set otherwise display will appear blank.
13. Check that LCD module has not been mishandled by applying excessive shock of mechanical stress which will cause the LC glass to misalign with the Elastomer strips that connect the LC glass to the PCB.
14. Check that LCD module has not been mishandled by applying excessive electrical stress in the form of electro-static discharge (ESD) or by applying reverse voltage to V_{DD} and V_{SS}. Always use electro-static handling precautions, grounded wrist straps and bench mats when handling LCD modules as they use CMOS LSI chips. Always use a grounded soldering iron when mounting connectors to the LCD module.
15. Check connections between EL backlight, DC-AC inverter, and the EL lamp mounted on the LCD module. Check input voltage to DC-AC inverter. Never operate the DC-AC inverter without an EL Lamp load, as this may damage the inverter. EL backlights dim with age and need to be replaced when their brightness level is no longer adequate.
16. Check that the correct series current limiting resistor for the LED backlight is in place between the power supply and the LED lamp. Check individual LCD module data sheets for maximum forward current, I_f, for LED backlight. The LED's may burn-out if the maximum forward current, I_f, is exceeded. Some, but not all, LED backlight modules will already have the current limiting resistor

on-board.

17. This problem is symptomatic of trying to use the 5x11 font selection when V_P<12 (section 8.2). Reprogram the Character Pitch Register so that V_P=12.

14.0 Internal Character Generator Font Pattern and Character Codes

Vmsb lsb >	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
2	blank	!	"	#	$	%	&	‘	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	¥	]	^	_
6	\	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	→	←
A	***	***	***	***	***	***	***	***	***	***	***	***	***	***	***	***
B	***	***	***	***	***	***	***	***	***	***	***	***	***	***	***	***
C	***	***	***	***	***	***	***	***	***	***	***	***	***	***	***	***
D	***	***	***	***	***	***	***	***	***	***	***	***	***	***	***	***
E	α	ä	ß	ε	µ	σ	p	g	√	-l	j	x	¢	£	ñ	ö
F	p	q	Ø	∞	Ω	ü	∑	Π	x	y				÷	blank	¦

*******Characters defined from A0 to DF is part of the Kanji character set. For a description of these characters please contact Hitachi or your local Densitron Corporation.

Note: Character defined from E0 to FF are part of a 5x11 font structure and will only work properly on an alphanumeric with the same LCD structure.

Amendment 001 to document AN-01

regarding mapping of VRAM in the LM3165 and LM4165

When programming the LM3165 or LM4165, special consideration must be given in the mapping of the VRAM to the LCD dots. Due to the nature of the HD61830, portions of the VRAM might not be visible on the display. The HD61830 can map up to a 128 x 240 dot format. Since the LM3165 and 4165 have a resolution of 128 x 128, the mapping is so that the first 112 memory allocations are off the left hand side of the LCD display. So when writing in the VRAM, both graphics and text, make sure you include this offset of 112 (or 19 for text).

There is another unique feature to the 128 x 128 that pertains to the mapping of the VRAM in character mode only. Not only is the offset still necessary, but the portion of memory usually left available for text is split in two. The first of these two portions is responsible for the odd rows of the display, and the second for the even rows. For example, to place the letter "A" (5x7) in the upper left hand corner of the display, you must place a 41H in memory location 0013H and in memory location 1013H.

This at first may appear that this mapping will double your code length, but this can be done simply in your subroutine responsible for clocking in data. After your text has been clocked into the specific memory allocation, add 1000H to this memory address and re-clock in the data again. Subtracting 1000H after this operation will put your counter back on track. This upper location of memory must also be cleared out when starting your text to eliminate garbage that is present in memory from boot up. The total portions of VRAM that should be cleared in text mode are locations 13H to 280H and 1013H to 1280H.
